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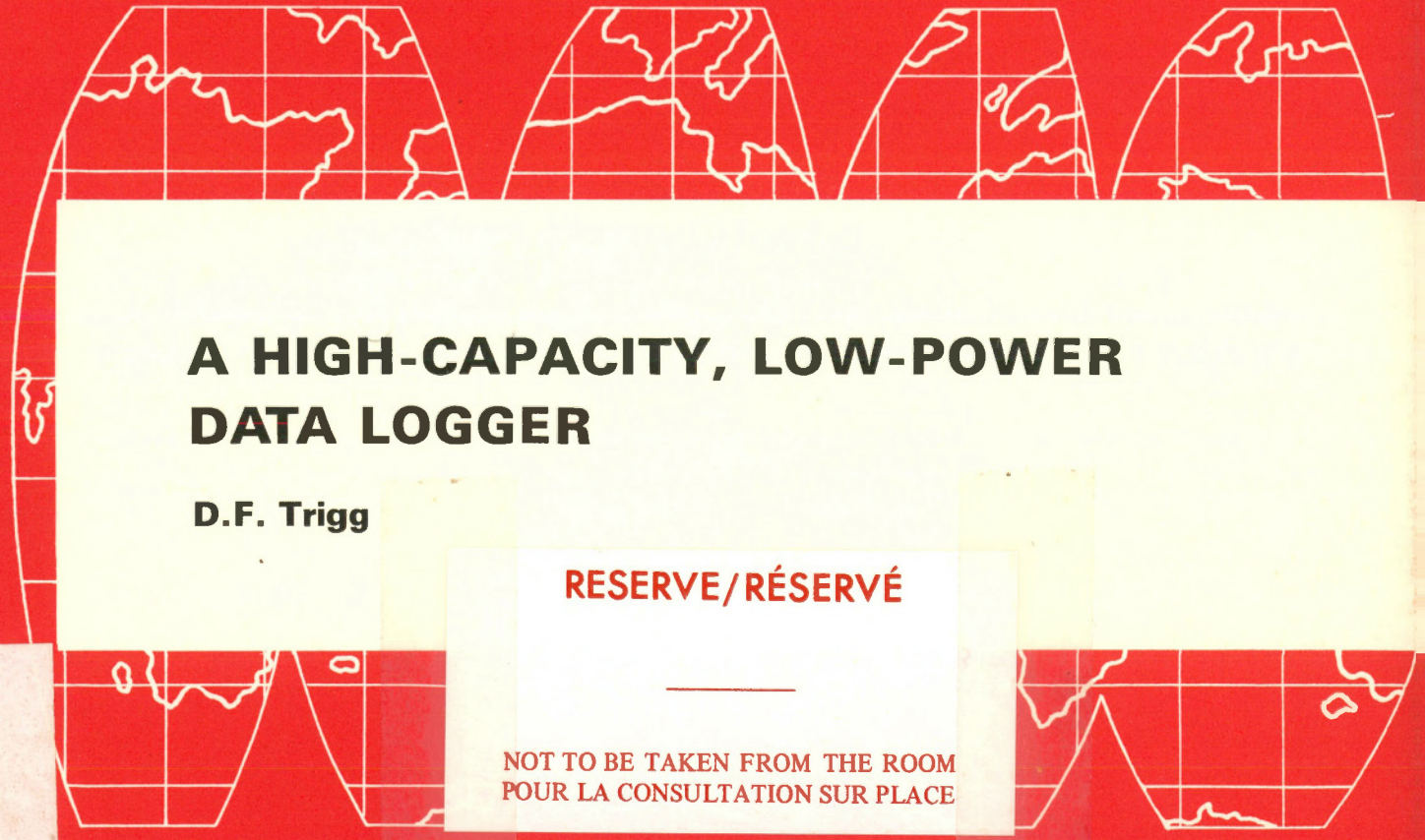

A HIGH-CAPACITY, LOW-POWER DATA LOGGER

D.F. Trigg

Geomagnetic Series Number 1
Ottawa, Canada 1975

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Contents

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D.F. Trigg

Abstract. A system capable of scanning and digitally recording data from up to 10 analog input channels is described. Input signals are converted to 12-bit binary words which are stored by a low-power 7-track incremental tape recorder capable of accommodating a 2,400 ft. reel of tape. Powered by internal batteries and consuming only milliwatts, the instrument is useful for recording geophysical data at remote sites, where it can remain in unattended operation for long periods.

Résumé. La présente étude donne la description d'un système capable d'explorer et d'enregistrer sous forme numérique les données analogiques de dix canaux d'entrée. Les signaux d'entrée sont convertis en termes binaires de 12 bits, accumulés sur bande par un appareil enregistreur d'accroissement à 7 pistes, à faible consommation d'énergie, et conçu pour recevoir une bobine de 2 400 pieds (800 m). A énergie de piles internes et ne consommant que quelques milliwatts, l'appareil est d'une grande utilité pour l'enregistrement des données géophysiques à des sites isolés, où il peut rester longtemps en opération sans surveillance.

Introduction

Geophysicists frequently find it necessary to acquire and store large amounts of data. Much of this work is complicated by the fact that sites of interest are remote from normal a.c. power sources. Analog recorders can meet the demand for low power consumption but their use creates problems in data reduction and storage, and so direct digital recording is looked upon with increasing favour.

With the commercial introduction of CMOS (complementary symmetry metal oxide semiconductor) logic devices[1], low-power digital data logging equipment became a reality. In particular, a 7-track, 200 bit-per-inch (BPI) incremental tape recorder which uses this technology became available and was adopted as the basis of this data logger. The recorder (Digi-Data model 1401 LP) can accommodate a 2,400 ft. reel of magnetic tape and so is capable of storing in excess of 3×10^7 binary bits of data. A one ampere-hour capacity 12 volt battery provides sufficient power for the writing of 600,000 tape characters (at 7 bits per character).

Another vital component which has recently become available in a CMOS version is an A-D converter. Several such 12-bit A-D converters are on the market, including the Datel model ADC-CM12B chosen for this application. Power is also conserved in the analog section of this device by interrupting power to that section except when it is needed.

The block diagram in Figure 1 depicts the general layout of the system. Dedicated alias filters provide preliminary input filtering for each of 10 analog input channels. This guards against the possibility of 'beats' between higher frequency input components and the system scan interval. One of the 10 inputs is selected by the analog MPX (multiplexor) and presented to the buffer, which provides a high input impedance to the analog MPX and a low output impedance to the A-D converter. The A-D converter output is a 12-bit binary number which is broken up into two 6-bit characters by the digital MPX and these are provided consecutively to the 7-track tape recorder. Scans of the inputs are initiated by pulses from a crystal-controlled oscillator which serves at the time standard.

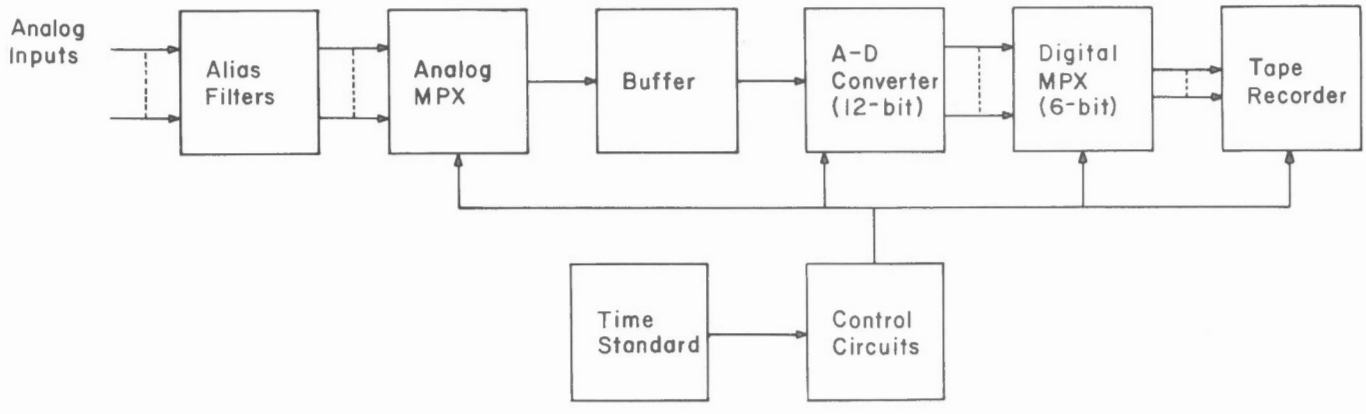

Figure 1. Block diagram of data logger.

Data format

Analog data from each input channel is written on magnetic tape as two consecutive 7-bit characters, with the seventh bit as parity (generated within the tape recorder). The first character contains the six most-significant bits (MSB) from the A-D converter and the second character the six least-significant bits (LSB). The data from 120 scans of the input channels forms one tape record. Thus, if only one channel is "scanned" the records will contain 240 characters but if all 10 channels are scanned the records will contain 2,400 characters. A standard inter-record gap (IRG) separates records on the tape and a standard end-of-file (EOF) mark can be generated when data acquisition is finished. Generation of an IRG takes four seconds, and therefore scans may not be initiated at any interval shorter than this. Neither time nor channel identification is encoded and written on tape.

Electrical specifications

Salient characteristics of the data logger are:

Number of channels	10
Input signal range	±10V
Input impedance (each channel)	>1M
Operating modes	Sequential scan only, short scan possible
Resolution	5 mV
Accuracy	0.1 per cent of full scale
Scan intervals	5, 10, 30 seconds
Time standard stability	±2 seconds/week (worst case)
Usable tape capacity	4.5×10^6 characters (3-channel scan)
Power consumption (mW)	$30 + \frac{\text{(characters written per hour)}}{40}$
Power supply	Internal NICAD battery, 15V, 8 A-H, trickle charged from 110V a.c.

Alias filters

As mentioned earlier in the text, input filters are necessary to prevent high-frequency signals at the inputs from appearing as a low frequency signal in the data by being heterodyned with the scan interval. The low-pass[2] alias filter of Figure 2 performs this function by greatly attenuating all frequencies whose periods are less than the scan interval. Gain G of the circuit as a function of frequency f is given by the expression:

$$G = [\,(\pi\sqrt{2}\,RC\,f)^4 + 1]^{-\frac{1}{2}}$$

where R and C are as shown in the diagram. Three of the components of the circuit have nothing to do with the frequency response but control other important parameters. The resistor in series with the inverting input is chosen to be 2R so that input bias current will not cause output errors. Provided $R \leqslant 700K$, output error due to input offset current will not exceed 14 mV (worst case). A 10K resistance in series with the non-inverting input prevents damage to the amplifier during power shut-down by limiting the current delivered by the capacitor into the input. The third component, a 10M resistor from the amplifier to V^-, sets the amplifier quiescent current to less than 30 μA so that 10 such filters demand no more than 300 μA from the supplies.

Analog MPX

The analog MPX in Figure 3 consists of an 11-bit serial-in parallel-out shift register, the outputs of which control CMOS analog switches to connect one of 10 analog inputs to the common analog output line. Prior to system operation a pulse on the 'initial clear' line resets the shift register so that only the first stage (a 4013) contains a 1. This stage turns on its related 2N5464 FET since $V_{GS} = 0$, and effectively connects the 'IN' terminal of the G150D analog switch to $V_{DD} = +15$ volts, turning the switch on. Analog input no. 1 is thus connected to the analog output line. All other switches are off since a logical 0 at the shift register outputs results in $V_{GS} = +15$ volts for the 2N5464's, turning them off and applying −15 volts to the 'IN' terminals of the G150D's via the 1M resistors.

After an A-D conversion and certain other operations related to processing channel 1 are completed a pulse is applied to 'bit select $\overline{Q}$', and this clocks the shift register. The 1 from the first stage shifts to the second stage and a 0 is shifted into the first stage, connecting analog input 2 to the analog output etc. Short cycling is accomplished by sampling a particular output stage of the shift register via the 10-position 'channel detect' switch and feeding the signal back into the 'delay' input. When that stage becomes 1 the delay flip-flop generates a pulse which resets the shift register. The resulting 1 at the first stage of the shift register is used as a 'stop clock' signal to tell the control logic that a scan is completed.

Switching transients in the analog MPX are not a problem because there is a long delay (≃25 milliseconds) between the time the MPX is advanced one channel and the time that the A-D conversion occurs on that channel. During this delay the information derived from the previous conversion is being written on tape.

Buffer, DC-DC converter

The output from the analog MPX is wired to the 'buffer in' of Figure 4, where the attenuated signal is presented to a non-inverting unity-gain operational amplifier. Attenuation is provided so that the 'scale factor' of the system is exactly 5 millivolts/bit, i.e. a full scale excursion from −10 volts to +10 volts at the input would change the A-D converter output by 4,000 counts (rather than 4,096). A capacitor at the buffer input provides high-frequency roll-off. It is chosen so that with a full-scale input excursion the capacitor will charge to within less than 1 LSB error in 25 milliseconds. A type 308A operational amplifier was chosen for the buffer for three reasons – insignificant input bias current, low input offset voltage and low quiescent power consumption. Errors introduced because of the bias currents and offset voltage are

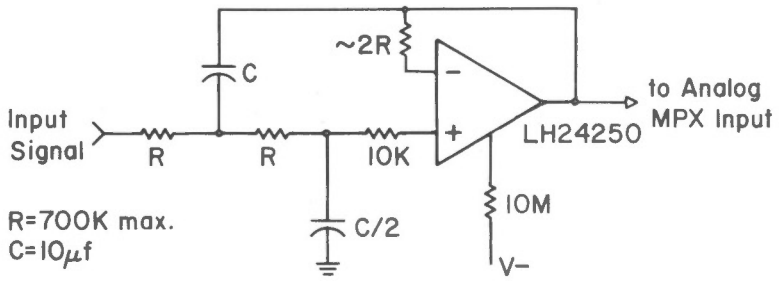

Figure 2. Alias filter for one input channel.

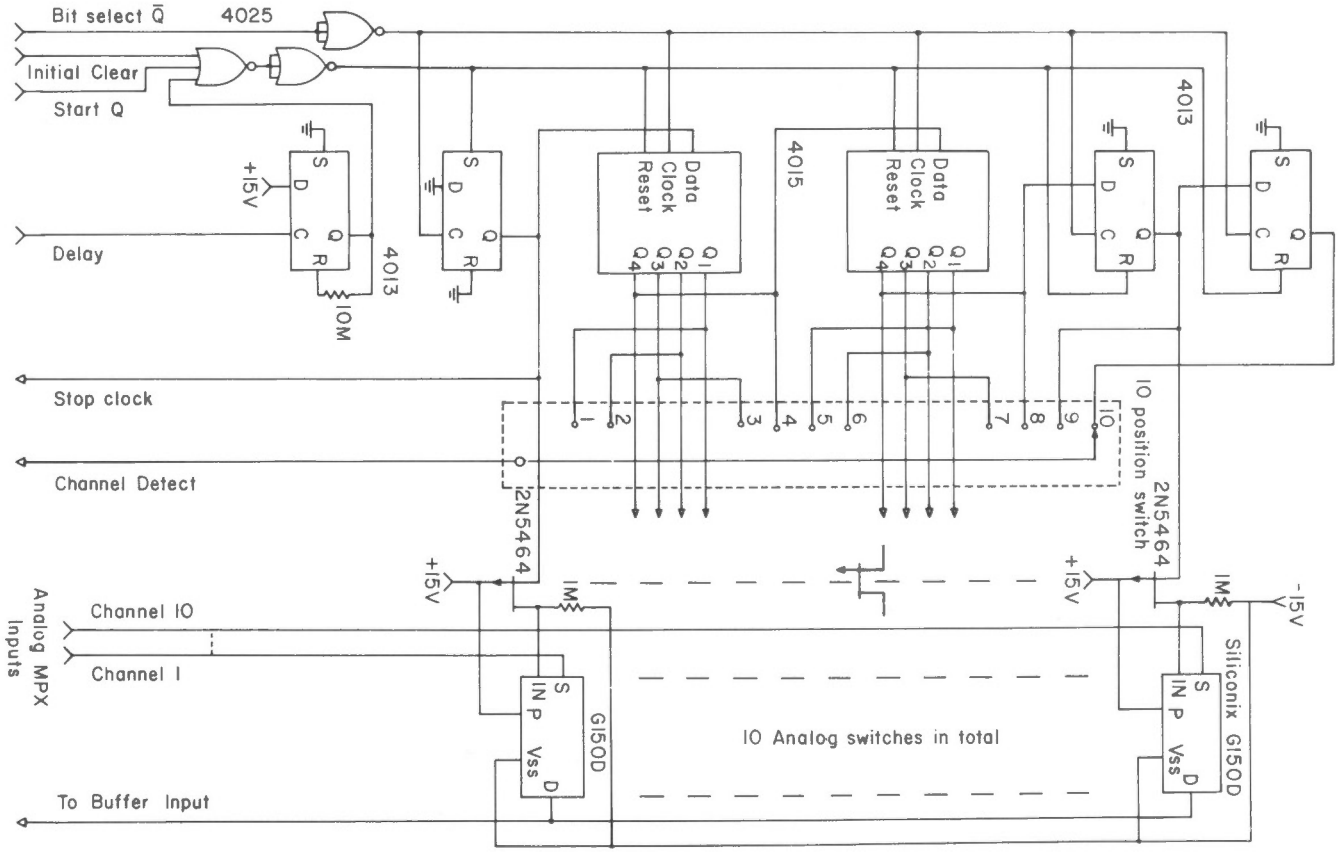

Figure 3. Analog multiplexor.

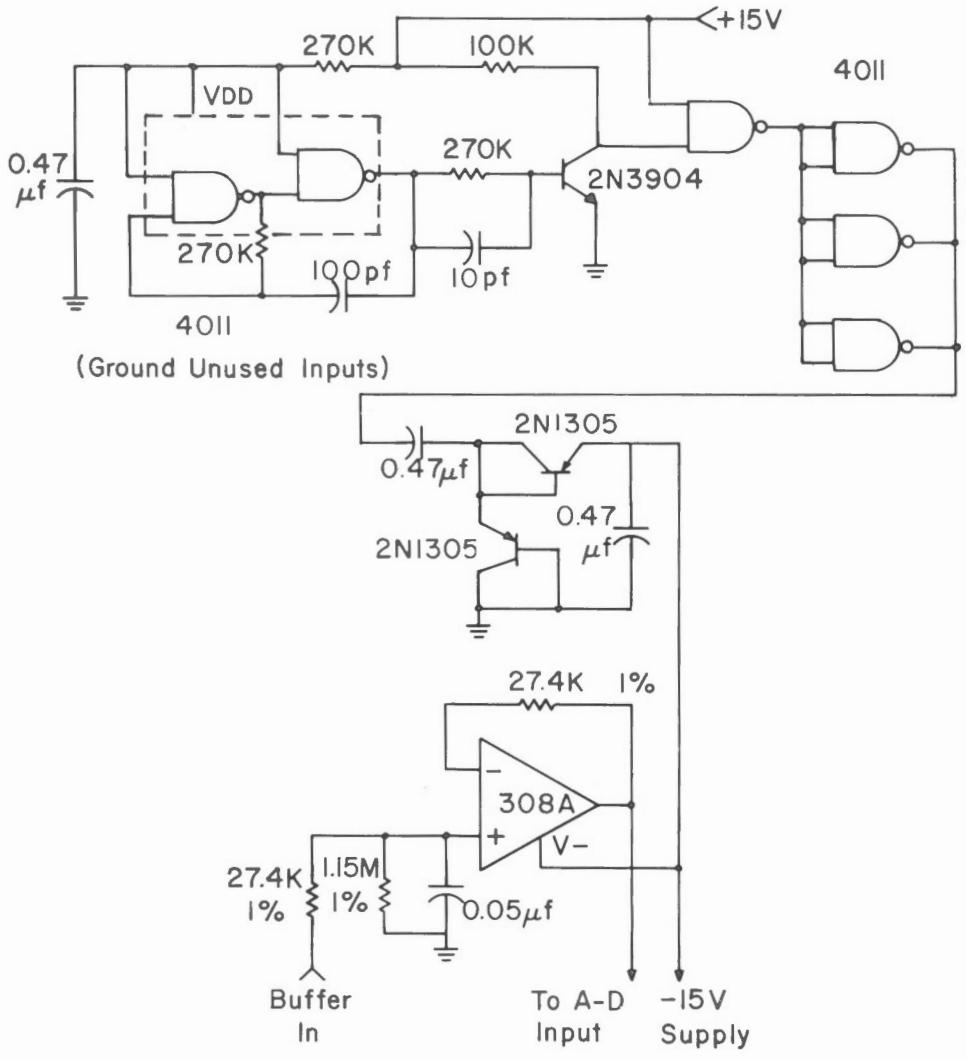

Figure 4. Buffer amplifier and DC-DC converter.

considerably less than 1 LSB. Current consumption in the 308A is a low 300 microamps from each supply. The buffer presents a high input impedance to the analog MPX at the frequencies of interest and a very low output impedance on its output line, which is the input to the 12-bit A-D converter (Figure 5).

Of all the data logger circuitry, only the buffer, the alias filters and the analog MPX require a negative supply and the total demand is less than 1 mA. A DC-DC converter obviates the need for a separate battery to meet that requirement. An astable multivibrator operating in the 10-20 KHz range is formed from a pair of NAND gates. It operates at about 5 volts supply obtained via a series 270K resistor to the +15 volt supply and a 0.47 μf shunt filter capacitor. This minimizes power consumption in the multivibrator. The remaining two gates in the package are unused. A 2N3904 transistor inverter converts back to 15 volt logic levels and drives three parallel NAND gate inverters. When the parallel inverter outputs are 1 the series capacitor charges, since one side is grounded by the 2N1305 operated as a diode. As the parallel-inverter logic level changes to 0 the 2N1305 to ground becomes reverse biased and the series diode-connected 2N1305 conducts to charge the output capacitor to -15 volts. When the parallel inverters return to 1 the series 2N1305 becomes reverse biased and the 2N1305 to ground is forward biased again and the cycle repeats. A DC-DC converter is thus obtained which is very efficient at low current levels. 2N1305 transistors are used as diodes because of their low forward voltage drop and attendant low losses.

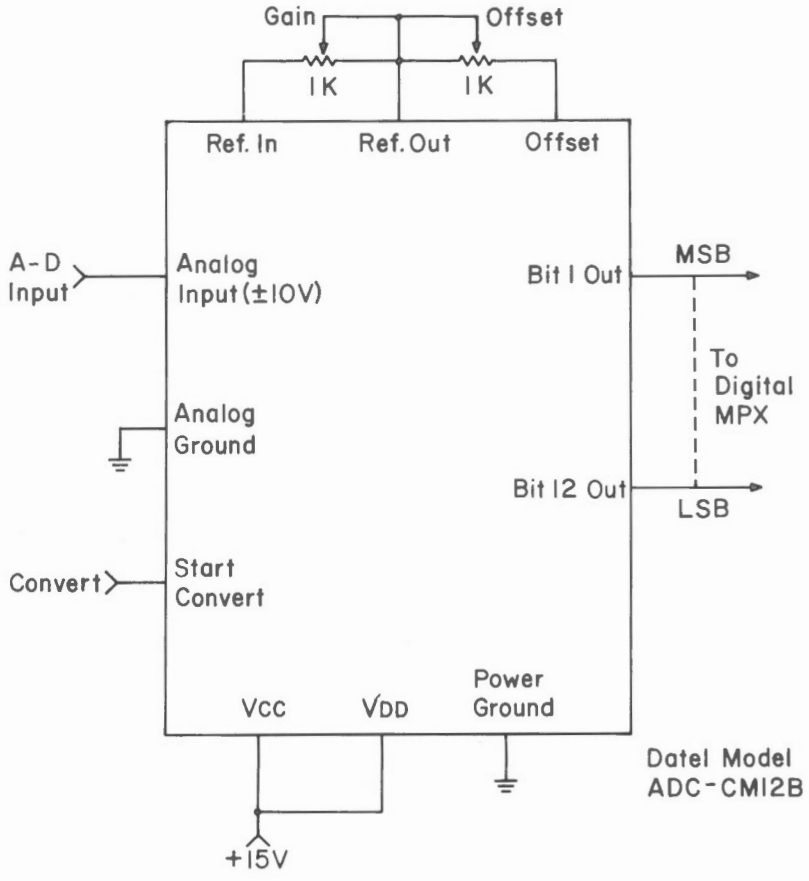

Figure 5. A-D converter connections.

Digital MPX

Digital MPX logic (4019's), shown in Figure 6, is provided to break the 12-bit parallel output word from the A-D converter into two 6-bit characters. These are written consecutively on the 7-track tape along with a parity bit for each character. Complementary 'bit select' signals select the six most-significant bits or six least-significant bits for presentation to the tape recorder inputs (Figure 7). If 'bit select' $\overline{Q}$ is 1, A-D bits 1 (MSB) to 6 are presented to tape recorder tracks B, A, 8, 4, 2, 1 respectively and if 'bit select Q' is 1, A-D bits 7 to 12 are presented to tracks B, A, 8, 4, 2, 1 respectively. The most significant character is written first. Parity is generated within the tape recorder, transmitted through the AND gate and written in track C. As no end-of-file (EOF) capability exists in the Digi-Data recorder, provision has been made to generate EOF in the control logic. The digital MPX has thus been provided with a 'write zeroes' line and a 'write ones' line for use in the EOF sequence. A 0 on 'write zeroes' inhibits data and presents all zeroes to all tracks. A 1 on 'write ones' forces a 1 to be written in tracks 1, 2, 4, 8 regardless of whether or not a 'write zeroes' command is present.

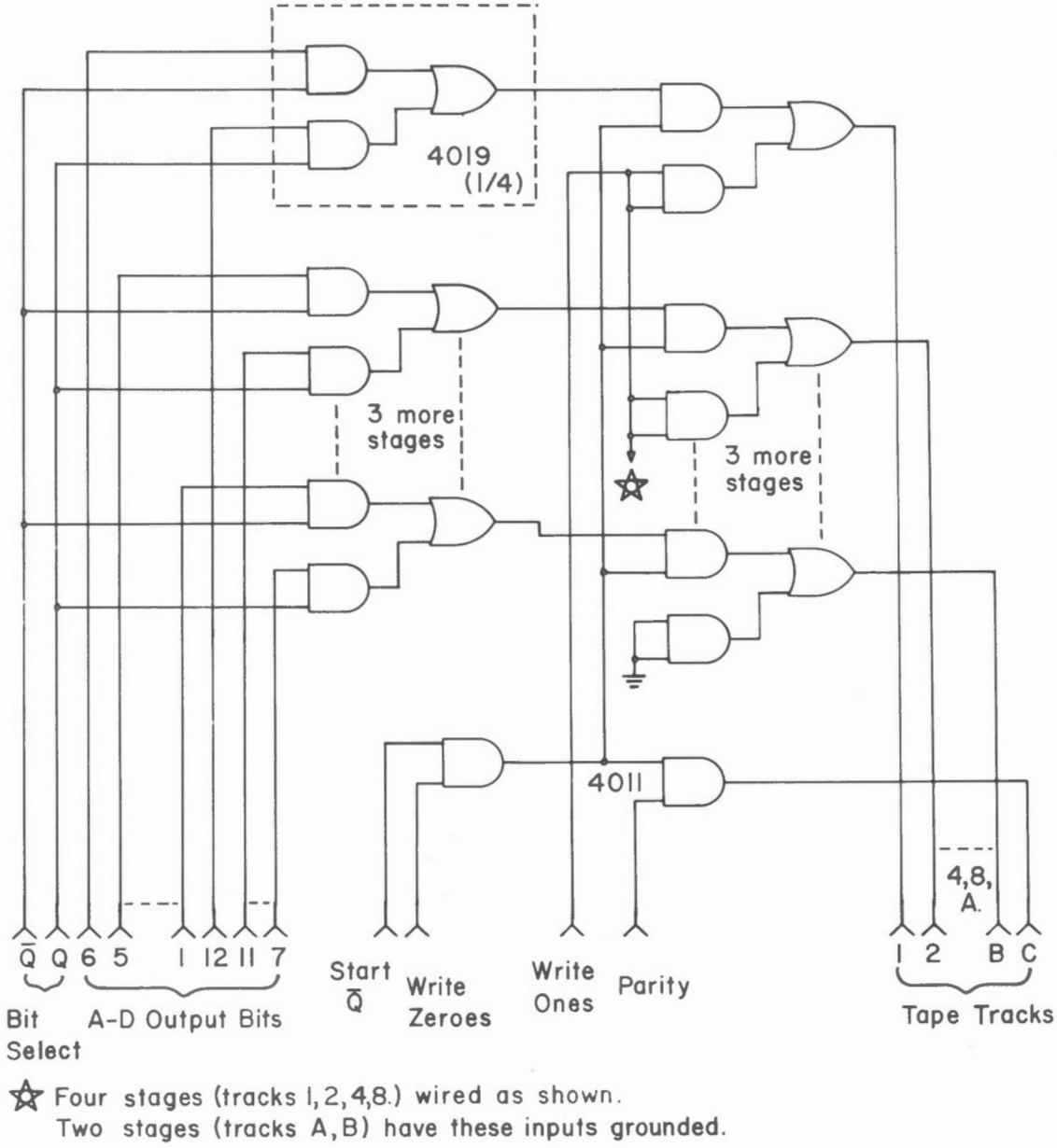

Figure 6. Digital multiplexor.

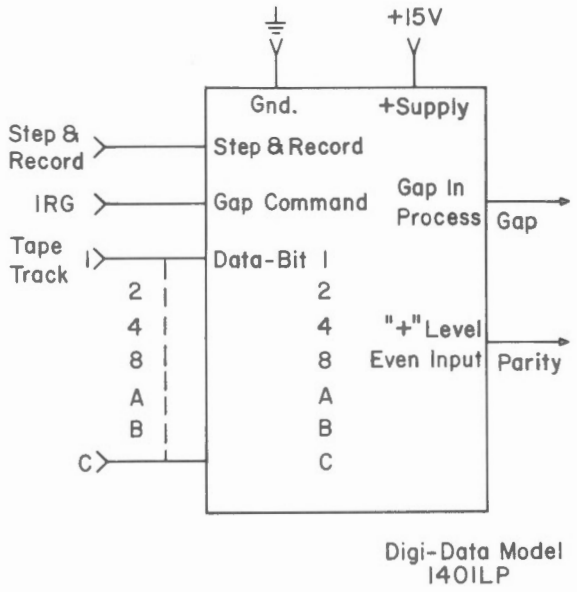

Figure 7. Tape recorder connections.

Start, stop, EOF

As an operating convenience the action of all control circuitry is inhibited at certain times by the 'start' and 'stop' flip-flop outputs (Figure 8). Specifically, the application of power to the system sets both flip-flops via 1 microfarad capacitors and 1N914 diodes in series, connected to their respective flip-flop set lines. Both these lines are returned to the Q output of a 50 microsecond pulse generator, which is normally 0, via 2.2M resistors. Power-up then results in an instantaneous logic 1 at the set lines, which return slowly to 0 as current flows through the 2.2M resistors. $\overline{Q}$ of the 'start' flip-flop is 0, inhibiting 'scan initiate' signals and Q is 1, holding various counters and flip-flops in their reset state. The state of the 'stop' flip-flop is such that it will not interfere with normal operation. When the 'start' switch is depressed the 'start' flip-flop is complemented and the control logic is no longer inhibited. Data scans can be initiated by applying pulses at the 'time' input from some time standard or by operating the 'manual scan' switch. When the system must be stopped the 'stop' switch is depressed, complementing the 'stop' flip-flop. Its Q output inhibits 'scan initiate' pulses and the $\overline{Q}$ output triggers the EOF sequence. The 'start' and 'stop' flip-flops are interconnected in such a way that after power-up a 'stop' command is ignored if it occurs prior to a 'start' command. Similarly, a 'start' command has no effect after a 'stop' command until the complete EOF sequence is finished, at which time both 'start' and 'stop' flip-flops are set again by the 50 microsecond pulse generator output.

Following a 'stop' command the 'clock enable' line is forced to 0, causing the data logger 'clock' in Figure 9 to run continuously until the current record is completed. At this time an inter-record gap (IRG) signal is sent to the tape recorder which responds by producing a gap on the tape and transmitting a 'gap' signal while this is in process. The trailing edge of this signal complements the 'zeroes' flip-flop (Figure 8) which gives a 'write zeroes' command to the digital MPX at the same time as it removes the reset from the 4020 binary counter. The 4029 up-down counter remains disabled by a logic 1 at its 'carry in'. Data logger 'clock' pulses continue and cause zeroes to be written on tape with each pulse until a binary count of 768 is detected at the Q_9 and Q_{10} outputs of the 4020. At this time the 'carry in' input of the 4029 becomes 0 and the 4029 begins to count clock pulses. When the count reaches 2 and again at 6 the 'write ones' line becomes 1, causing ones to be written in tape tracks 1, 2, 4, 8. When the count reaches 8 the 4029 input pulses become inhibited. The system clock continues to run until a count of 1024 is detected at Q_{11} of the 4020, and during this time zeroes are written in every track. Q_{11} becomes 1 at the 1024 count, disabling the system clock and causing a pulse to be generated by the 50 microsecond pulse generator. 'Start' and 'stop' return to their power-up configuration and the system is halted. In summary, the result has been the completion of the current record, followed by a record gap and an EOF mark. The EOF was comprised of 769 tape recorder steps of blank tape ($\simeq 3\frac{3}{4}$ inches at 200 steps per inch), followed by an octal 17, three more blank characters, another octal 17 and a further 248 steps ($\simeq 1\frac{1}{4}$ inches) of blank tape.

Control

The control circuit of Figure 9 is centred around a 40 Hz system 'clock' or astable multivibrator from which are derived appropriate 'convert' commands to the A-D converter, 'step and record' and 'IRG' commands to the tape recorder and 'bit select' commands to the digital MPX. Under normal conditions the clock, formed from a type 4001 NOR gate package, is held inhibited with its output at 1 by a signal from the equivalent of a 5-input AND gate. The five AND gate inputs are 'clock enable', 'stop clock', '$\overline{\text{initial clear}}$', 'bit select' Q and 'clock'. 'Clock enable' has been described earlier and remains 1 at all times except during the EOF sequence, and so has no relevance to the sequence of events to be described now.

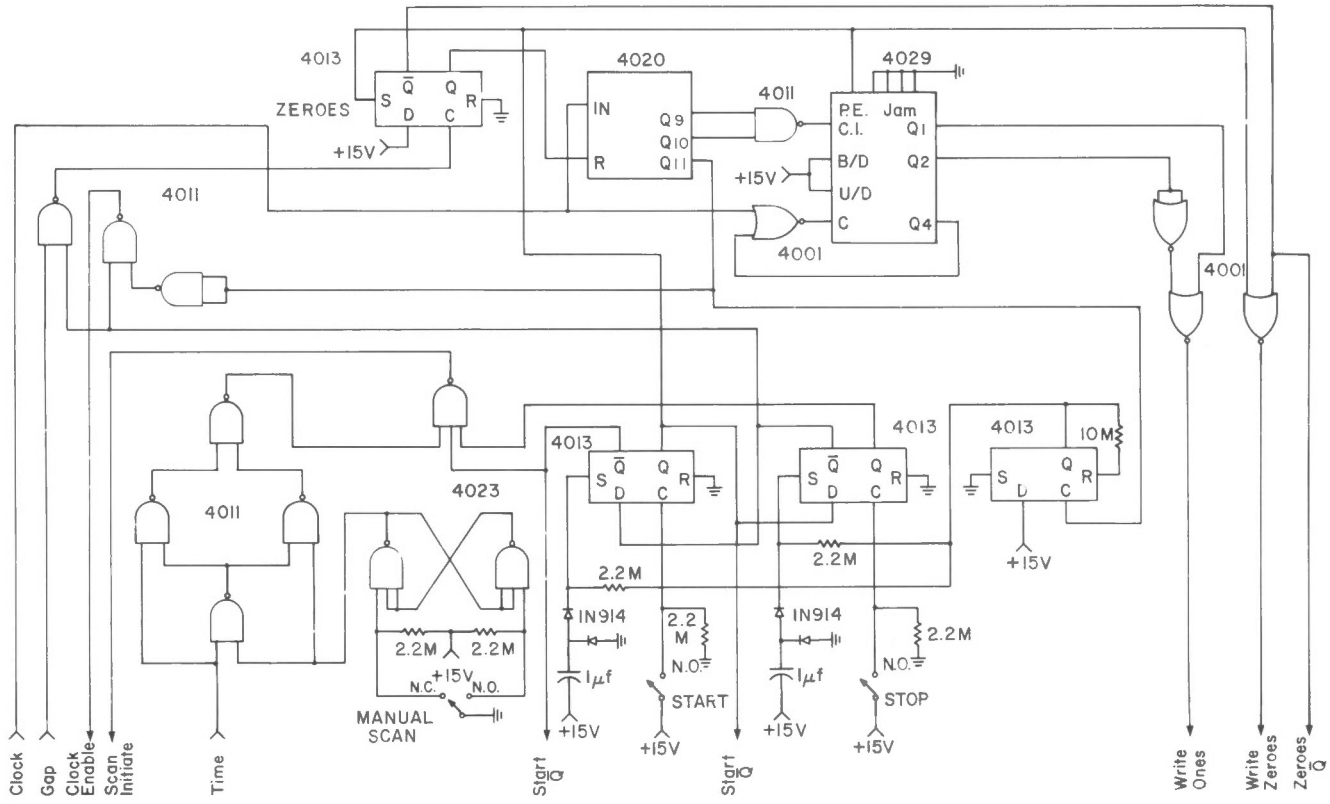

Figure 8. Start and stop circuits and EOF generator.

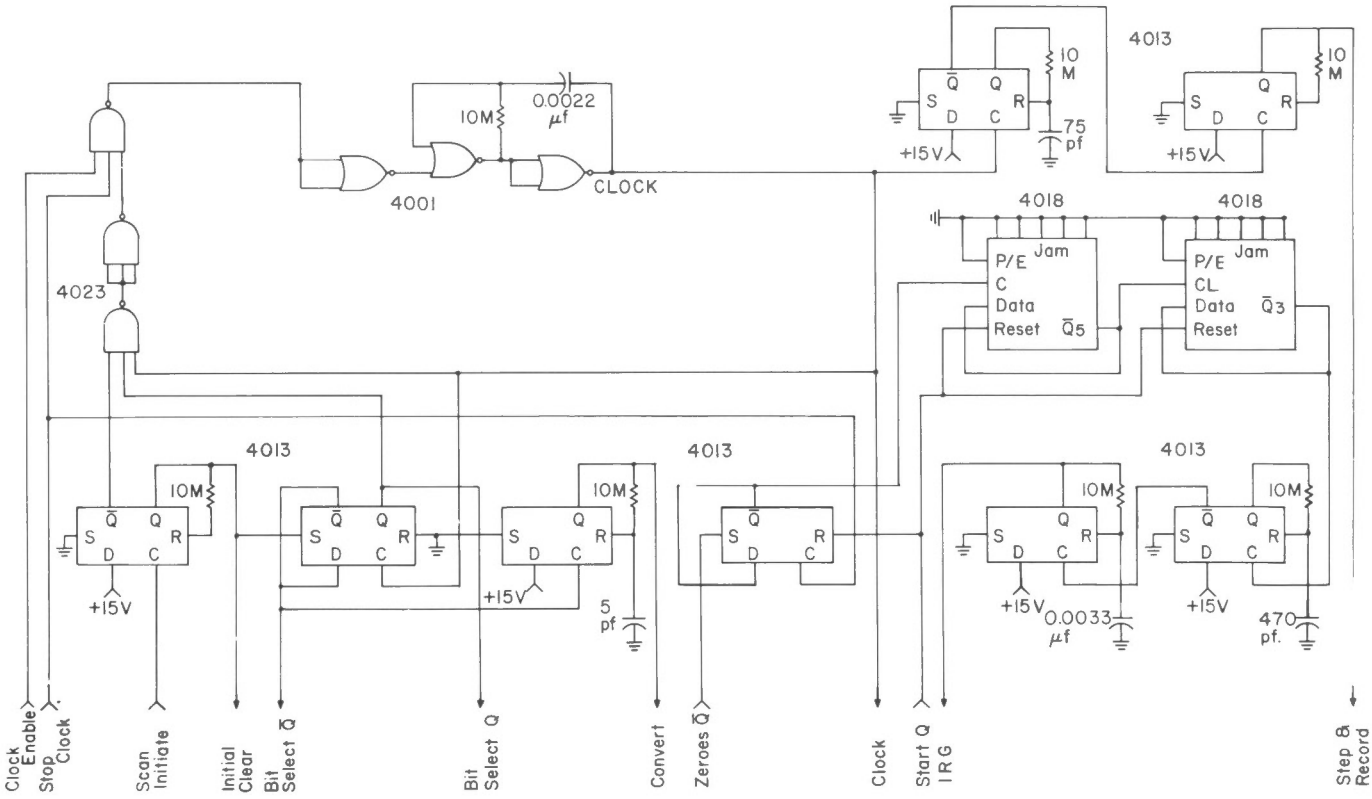

Figure 9. Control circuit.

A scan begins when a +ve edge occurs at 'scan initiate', causing an 'initial clear' pulse to be generated (50 microsecond duration). Initial clear forces the clock output to 0, which ensures the continuation of events since 'clock' is also an input to the AND gate, and any input 0 will keep the clock running. When the clock returns to 1 it complements the bit select flip-flop (see timing diagram Figure 10) which then holds its Q output to the AND gate at 0 as well as selecting the most-significant bits in the digital MPX. The accompanying +ve edge at $\overline{Q}$ triggers a 100 microsecond pulse generator which sends a 'convert' command to the A-D converter. This conversion is complete within 160 microseconds. Meanwhile, the same +ve edge at clock has triggered a 500 microsecond delay (all figures are approximate) to allow ample time for completion of the conversion before this delay triggers a 50 microsecond pulse generator to send a 'step and record' command to the tape recorder. The next +ve edge at 'clock' complements 'bit select' once more, selecting the A-D least-significant bits. A -ve edge thus occurs at 'bit select' $\overline{Q}$ which advances the analog MPX one channel. The -ve edge at $\overline{Q}$ has no effect on the 'convert' pulse generator, so that an A-D conversion does not occur at this time. After the 500 microseconds delay the A-D least-significant bits are written on tape. The cycle is now complete for the first channel and the system continues to convert channels until such time as the 'stop clock' signal is received from the analog MPX. Once this is received the system halts as all inputs to the AND gate in due course become 1, stopping the system 'clock'.

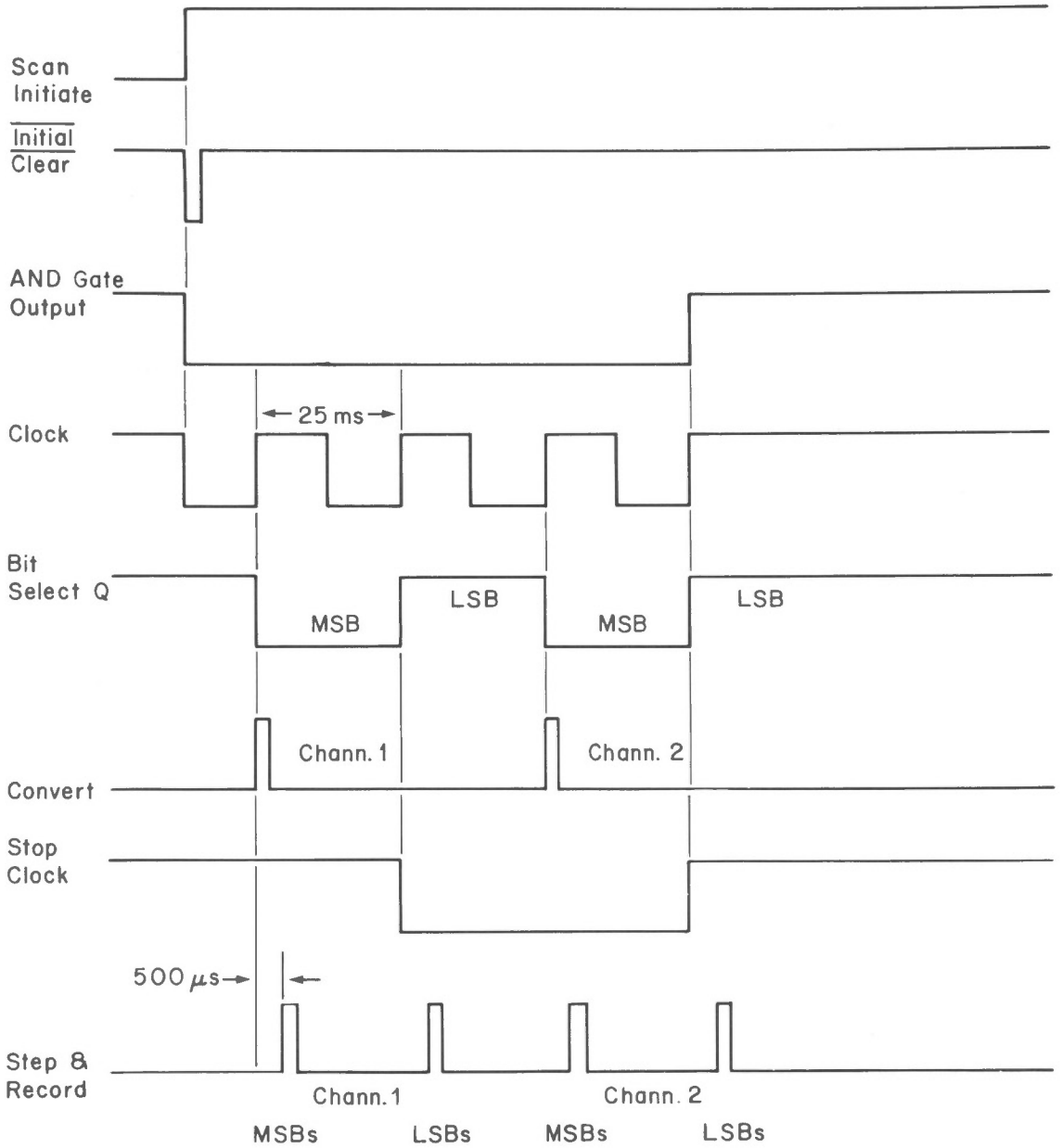

Figure 10. System timing diagram — two channel scan.

'Stop clock' signals are counted by dividing by factors of 2, 10 and 6 respectively using a 4013 flip-flop and two 4018 counters. When this total of 120 scans is reached a 3 millisecond delay is triggered (sufficient time to ensure that the tape recorder receives the final 'step and record' command) which in due course triggers a pulse generator to send an IRG command to the tape recorder. The tape recorder ignores the IRG until it has finished its execution of the final 'step and record' command, a process that takes about 17 milliseconds to complete. Hence, the IRG pulse must have a duration longer than this and in fact it lasts approximately 23 milliseconds.

Time reference

Time signals are derived by division of the output frequency of a 2,097,152 Hz crystal-controlled oscillator[3] shown in Figure 11. As this is the only portion of the system which operates at high frequency, steps have been taken to minimize the power consumption of this circuit. The 4045 is a package containing the inverters necessary for the oscillator and also a 21-stage binary divider. It is operated at 5 volts supply obtained from +15 volts via the 1N5297 current regulator diode (1 milliamp.) and the LM103 zener diode. The LM103 can operate at very low current, leaving most of the 1 milliamp. available to the 4045, if needed, while maintaining the supply voltage to the oscillator constant.

Unfortunately the 4045 has no reset capability, so that resetting all the external circuitry would still leave a 1-second uncertainty in the time. The 1-second output is a pulse of 30 milliseconds duration, which provides a means of escape from this uncertainty. When Q of the 4013 'reset' flip-flop becomes 1 at the 'reset' command this signal is applied to an input of gate A via a 1M resistor. Nothing happens until the 1-sec line of the 4045 goes briefly to 1, at which time gate A (operated from 5 volts) interrupts power to the oscillator portion of the 4045. The 4045 can thus be made to stop somewhere in that 30 millisecond interval when its output is 1. When 'reset' is removed a finite time is required for the oscillator to restart but the total uncertainty in time is reduced to something of the order of 100 milliseconds – an acceptable value for most applications.

The 1- second output of the 4045 is converted to a 15 volt logic level by a 2N3904 transistor and re-inverted by one stage of gate B. Further processing is simply a matter of division by factors of 5, 2 and 3 using a 4018, 4013 and 4027 respectively. Type 4001 NOR gates ensure that a +ve edge will never occur on the output line when 'reset' is applied and will always occur when 'reset' is released.

Power supply

Figure 12 shows the data logger power supply. NICAD batteries were chosen as the power source in order to satisfy several stringent requirements. Foremost among these is the need for portability. The unit is primarily intended for use at remote sites where 110 volt power is not available, and great stress has been placed upon minimizing power consumption.

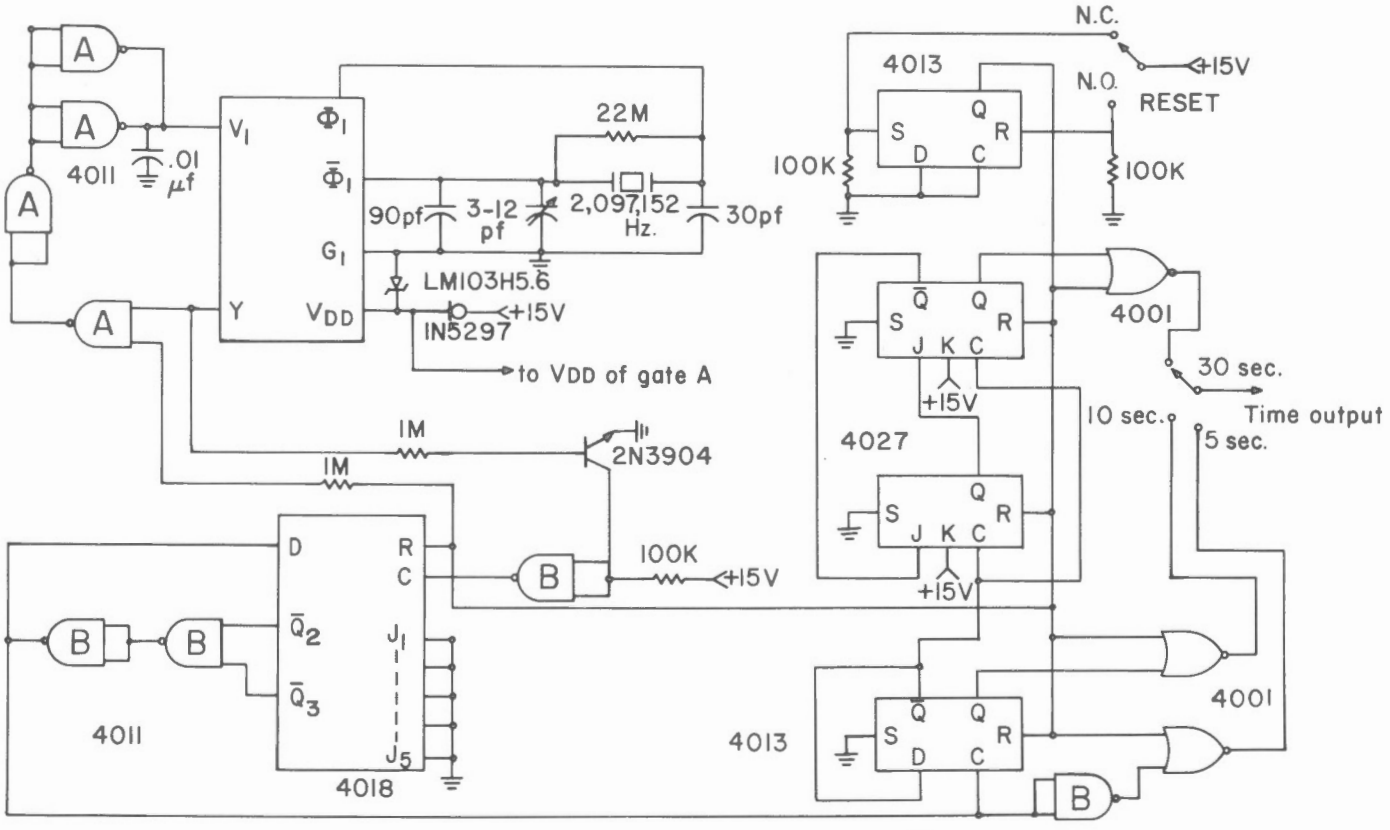

Figure 11. Time reference oscillator circuit.

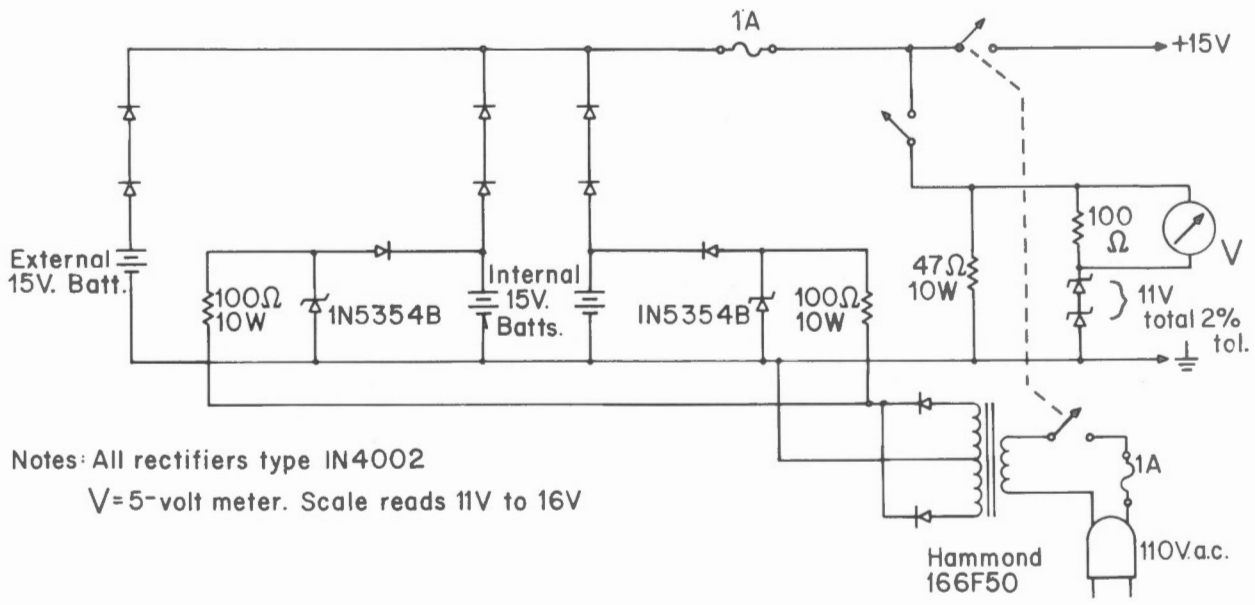

Figure 12. Power supply.

Although the average power consumption is extremely small there are periods when the supply must deliver current pulses of nearly 300 mA while maintaining good voltage regulation. NICAD batteries are ideal in this situation because of their very low internal resistance. Another requirement is that the supply must remain in the range from 12V to 15V over the entire battery discharge cycle. Again, NICAD batteries can meet this requirement nicely because of their flat discharge characteristic.

Provision has been made to accommodate two completely independent internal batteries and an external battery. Normally only one battery would be in use, but all three could be connected without harm because of the decoupling diodes. The battery with the highest output voltage automatically supplies the load. This feature is useful when a low battery must be replaced without interrupting system operation. One simply connects the fresh battery to the system and then removes the spent battery for recharging. Two series-connected diodes were used to decouple each battery in order to drop the voltage of 12 'D' cells (convenient for physical reasons) so the supply would not greatly exceed 15 volts.

Independent trickle chargers operating from a common transformer can maintain the internal batteries fully charged when line power is available. 17V zener diodes prevent damage from overvoltage if the batteries should be removed while the line power is connected. A 1A fuse affords battery protection against an accidental short circuit. The battery can be tested under realistic load conditions by depressing the 'battery test' switch. The associated voltmeter will give a zero reading unless the battery delivers more than 11 volts under load.

Tape processing

Low-density recording makes good sense in field operations because of loose tolerances on character spacing, skew etc. The prospective user of the data loggers should, however, give some thought to the problem of processing the 200 BPI tapes. Computer facilities are generally designed to handle 556 BPI or 800 BPI tapes which have been produced in a laboratory environment. 200 BPI tapes produced in the field with the inevitable parity errors, short and long records and various other defects are handled with some difficulty, if at all. Our experience in the Geomagnetic Division indicates that editing and transcription of such tapes should be done in-house if at all possible.

Performance

A prototype data logger was constructed in 1972 and tested under field operating conditions in 1972 and 1973. Results obtained at that time indicated the need for alias filters, which were subsequently included in the instrument. Although equipment failures occurred, they could often be attributed to factors such as poor batteries or operator errors. The performance was sufficiently encouraging that a commitment was made to have four data loggers produced commercially. These units have performed very unreliably. In nearly every instance, malfunctions have been traced to defective operation of the tape recorders. No single component is consistently at fault, but trouble has at one time or another been encountered with pinch roller arms, tension arm switches, reel motors and integrated circuits. Up to the time of writing these difficulties have prevented the successful use of the data loggers in field experiments. Hopefully these problems will eventually end and the data loggers can then be expected to meet their full potential for low-power data acquisition.

References

[1] Motorola Semiconductor Products Inc., 1974, McMOS Handbook.
[2] Trigg, D. 1972. An amplifier and filter system for telluric signals, Pub. Earth Physics Branch, Vol. 44, No. 1, p. 2.
[3] Eaton, S.S. Micropower crystal-controlled oscillator design using RCA COS/MOS inverters, RCA Application Note ICAN-6539.