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# ENERGY, MINES AND RESOURCES

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# *TECHNICAL MANUAL FOR A FIVE DIGIT BCD INTERFACE DESIGNED FOR USE WITH A MONROE 1666 CALCULATOR*

by

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# TECHNICAL MANUAL FOR A FIVE DIGIT BCD INTERFACE DESIGNED FOR USE WITH A MONROE 1666 CALCULATOR

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## SUMMARY

An instrument package developed to transfer data from an NS600 pulse height analyser to a Monroe programmable calculator is described.

The electronic circuits convert parallel data to the appropriate serialized code with required additional function commands. In addition, the unit continually displays input data on "LED" devices.

The system employs integrated circuits and optoelectronic devices.

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# INTRODUCTION

The prototype interface to be described was designed and constructed to improve the data reduction capabilities of Gamma-ray and X-ray instrumentation used by the Spectrochemistry Group of the Mineral Sciences Division.

In the original equipment, a pulse height spectrum was accumulated and stored in a Northern Scientific NS-600 pulse height analyser. The full spectrum was then printed out on a high speed parallel printer which displayed the number of counts in each channel. The printout sheet was examined and selected data was manually keyed into a Monroe 1666 programmable calculator.

The interface herein described allows the calculator to obtain data directly from the pulse height analyser. Data selection and calculations can now be carried out automatically by means of calculator programs.

In addition, the interface displays channel data up to five decades on "LED" numerical displays, controls the channel advance of the analyser and contains manual gating of the data transfers so that the analyser data may be examined while data output to the calculator is inhibited.

## GENERAL DESCRIPTION

The digit sequencer interface (Fig. 1) allows a Monroe 1666 programmable calculator to accept up to five decades of data presented in BCD parallel logic. Although the interface was primarily constructed to couple the calculator to an NS600 multichannel analyser it can be used with other devices equipped with BCD outputs.

The interface consists of four circuit boards; a level board, a sequence board, a display board, and a channel advance control board.

Input data is examined and presented to the calculator in $\overline{BCD}$ form, one digit at a time, commencing at the most significant digit. While each digit information is present at the calculator input an $\overline{ENTER}$ command is generated. When all the digits of the number have been sequenced into the calculator entry register, a $\overline{RESUME}$ command is generated to direct the calculator to operate on the acquired data.

The display circuit continually examines the BCD input data. This data is code converted into a seven segment code and the numerical data is displayed on LED displays located on the front panel. It should be noted that data is displayed regardless of the output mode of the interface. The operator is able to examine input data while the interface output is inhibited.

When servicing the interface, there can be a malfunction of the interface with proper data display so it should not be assumed that output data is being presented because there is data display.

The input lines of the parallel BCD data are connected through the edge connector of the level board. Each line presents its logic level through a 2N1306 input transistor. Each of the twenty input circuits is wired as a non-inverting emitter follower circuit. The emitter output presents data to both the decoder display and the digit select circuits of the interface.

The timing generator circuits, located on the sequence board, generate all the appropriate command pulses to transfer data to the calculator in proper sequence (Fig. 1). A positive level at the sequence board edge connector (pin 36) starts the timing generator. The generator will go through one complete

cycle transferring five digits of information and generating an $\overline{\text{ENTER}}$ pulse during the time each $\overline{\text{BCD}}$ digit code is present at the output, and generates a $\overline{\text{RESUME}}$ pulse after all five digits have been sequenced at the output. The timing generator will then halt until another positive level command is received.

All output circuits to the calculator are electrically isolated from the interface by means of optically coupled data transfer modules consisting of a light emitting diode and a phototransistor detector encapsulated in an IC in-line package (MCT-2).

## PHYSICAL CHARACTERISTICS

The data sequencer interface is housed in a Hammond 1426J low silhouette cabinet. The operating controls and the LED data input displays are mounted on the front panel.

Electronic circuit components consisting of integrated circuits and discrete components are mounted on four sub-chassis. Two different packaging techniques have been employed to offer the most efficient use of the available cabinet geometry.

Two plug-in Vero boards (D.I.P. board part No. 11823) have been employed for the data select and the level converter circuits. The board connectors are mounted on a bracket assembly bolted to the main chassis. The boards are designated selector board (nearest main chassis) and converter board.

The data display board is fixed to the front panel. The display board employs pre-punched "Vectorbord" and conductive circuit sub-elements mounted on thin substrates which have a pressure sensitive adhesive backing ("Circuit-Stik").

The channel advance circuitry is located on the fourth sub-assembly mounted under the main chassis.

A commercial power supply module has been used to supply the five volts DC level to operate the system. All input and output data lines are connected to the Vero connectors and are housed in the two multi-conductor cables connected through the rear of the instrument package.

## CIRCUIT FUNCTIONS

### A. Start Circuit

The start circuit is enabled by an external positive pulse. The Schmitt-trigger input circuit allows jitter-free triggering from positive levels with transition rates as slow as one volt/second. The start input requires a positive-going 1.5 volt level to trigger. When triggered the output $\overline{Q}$ (pin 1) switches to ground for a period of approximately 20 μ seconds. The period is set by the timing capacitor between pins 10 and 11. The zero state at $\overline{Q}$ of the 74121 is connected through the inhibit gate to pin 1 of a 74196 presettable decade counter. The zero or ground state on pin 1 forces a preset BCD count of three at the four level outputs. While pin 1 is at ground the clock input, pin 8, is inactive.

### B. Inhibit Circuit

This circuit (Fig. 6) allows the pulse height analyser to be stepped through channels without transferring data to the calculator. The circuit blocks start pulses at output of the 74121 so that the start sequence cannot be generated. The gate is controlled from the front panel toggle switch "INHIB". The circuit has been constructed from 2 NAND gates of a 7400 integrated circuit. One of the NAND gates is wired as an inverter for the input signal. The output of this inverter is connected to one input of the second dual input NAND gate. The other input is connected to the common terminal of a SPST toggle switch (INHIB switch). The logic of this circuit permits a ground state at the output NAND when both inputs are in the 1 state. If the INHIB switch is connected to VCC then the output state will follow

the input signal, but if the INHIB switch is connected to ground, then the output will always remain in the 1 state.

## C. Clock Circuit

The pulses required to step the sequencer through one complete cycle are generated by the clock circuit. The clock pulses commence when the start circuit presets the 74196 counter and stop when the RESUME command is produced at the end of the data enter sequence. The clock circuit is then out of action until another start command pulse is received.

The clock pulses are generated from an NE555 integrated circuit wired as a free-running multivibrator. The frequency is determined by the sum of the 1K resistor from VCC to pin 7, the 270K resistor between pins 2 and 6 and the external timing capacitor from pin 6 to ground. The resistance ratio of the two resistors sets the duty cycle of the output pulse. The multivibrator is controlled by supplying power to the module from pin 1 of the 7442 BCD-to-decimal decoder.

## D. Counter Circuit

The serial clock pulses generated from the NE555 are accumulated in the counter circuit. The circuit employs a 7473 JK flip-flop input and a 74196 presettable binary counter. Both the 7473 and the 74196 step on the negative edge of the input pulse. The output of the counter circuit presents the accumulated number of clock pulses in BCD 4 level code.

The divide-by-two flip-flop is required in order to time slot the generation of the $\overline{\text{ENTER}}$ command (see pulse time sequence diagram Fig. 2).

The counter sequence commences on receiving a negative start pulse. The ground state of this signal sets the Q output (pin 12) of the 7473 at ground and BCD three on the 74196 output lines. The counter receives clock pulses until BCD zero has been

scaled into the 74196. At this point the clock is turned off
until another start command is received.

### E. Sequence Circuit

This circuit (Fig.4) presents time sequenced command
signals to the digit select circuits, controls the operation of
the clock and generates the $\overline{\text{RESUME}}$ command required by the cal-
culator. The basic circuit consists of a 7442 BCD-to-decimal de-
coder. This module interprets the BCD code presented to the four
input lines by the counter circuit. When a BCD number is pro-
grammed to the input, the appropriate one out of ten outputs is at
ground and all other outputs are at +5 volts.

The power for the clock circuit is connected to the
BCD zero (pin 1) output so that, when the sequencer decodes BCD
zero from the counter circuit, the zero output switches to ground
and the clock circuit is off. When a start command is generated,
the counter circuit loads BCD three to the input lines of the
7442 and pin 1 switches to +5 volts. The clock is energized and
the counter accumulates clock pulses. The outputs step though
ground states to control the digit select circuits. The digit
select commands are inverted to produce the required logic at the
NAND gate inputs. The output for the BCD number nine is directed
to the calculator as the $\overline{\text{RESUME}}$ pulse. When the sequencer reach-
es BCD zero pin 1 again goes to ground and the clock is turned
off.

### F. Digit Select Circuit

The digit select system of the interface examines the
BCD form to the common four level output lines. The system re-
quires five similar basic circuits, one for each digit.

Each basic digit circuit consists of four two-input
NAND gates housed in one IC package, type 7403. One input of each
gate examines an appropriate line of the BCD information present-
ed to the interface. The other four inputs are wired parallel

and connected to one of the outputs of the digit select inverters. As the 7442 steps through its sequence a "one" level will appear on the common line of the selected digit circuit. If the other input is in the "one" state (determined by the input data presented) a ground state will appear at the output during the time a select pulse is present. The outputs of the five digit circuits are tied to common 4 wire lines designated $\overline{K8}$, $\overline{K4}$, $\overline{K2}$, and $\overline{K1}$. The BCD input information is time sequenced on the common lines in $\overline{BCD}$ form commencing at the most significant digit.

## G. Input Driver Circuits

The level board contains 20 input circuits (Fig. 3) to accommodate BCD information for five digits. Each of the identical circuits consist of a 2N1306 transistor connected as an emitter follower. The input circuits allow the interface to accept BCD levels of from +4 to 15 volts. The series diodes were installed to protect the input if the interface was accidentally plugged into external equipment with negative logic.

## H. Isolator Circuits

Since the circuit ground of the calculator is at -15 volts with respect to chassis ground, the calculator lines are optically coupled to the interface to prevent any accidental shorting of the floating supply. The optical couplers are Monsanto MCT2 photo transistor diode units. The anode of the light emitting diode is wired through a 1K ohm resistor to VCC. The level line is connected to the cathode. When the level goes to ground, the diode conducts, switching the phototransistor on. The transistor shorts the calculator line to VDD. The unit operates as a non inverting coupler so that a ground state on the input line produces a ground state on the calculator line.

I. $\overline{\text{ENTER}}$ Circuit

      While BCD data is on the $\overline{\text{K8}}$, $\overline{\text{K4}}$, $\overline{\text{K2}}$ and $\overline{\text{K1}}$ lines of the calculator it is necessary to generate a negative level on the $\overline{\text{ENTER}}$ calculator terminal. The interface circuit uses a 7410 integrated circuit. The IC houses two three input NAND gates. One gate is wired as a simple inverter. The second gate generates a negative level when the clock is high. This gating permits a negative pulse during the time each digit BCD data is present. Note that the $\overline{\text{ENTER}}$ pulse is inhibited during the generation of the $\overline{\text{RESUME}}$ pulse.

J. Channel Advance Circuit

      This clock circuit (Fig. 5) supplies negative five volt pulses through the INTERLOCK connection of the NS600 to control the channel advance of the analyser. The clock pulse is generated by the 2N1671 unijunction. The RC time constant at the emitter connection determines the pulse frequency. A manual start-stop and speed-select are incorporated in the circuit. The oscillator pulse is inverted in the 2N731 transistor driver circuit to supply the appropriate negative channel advance pulse.
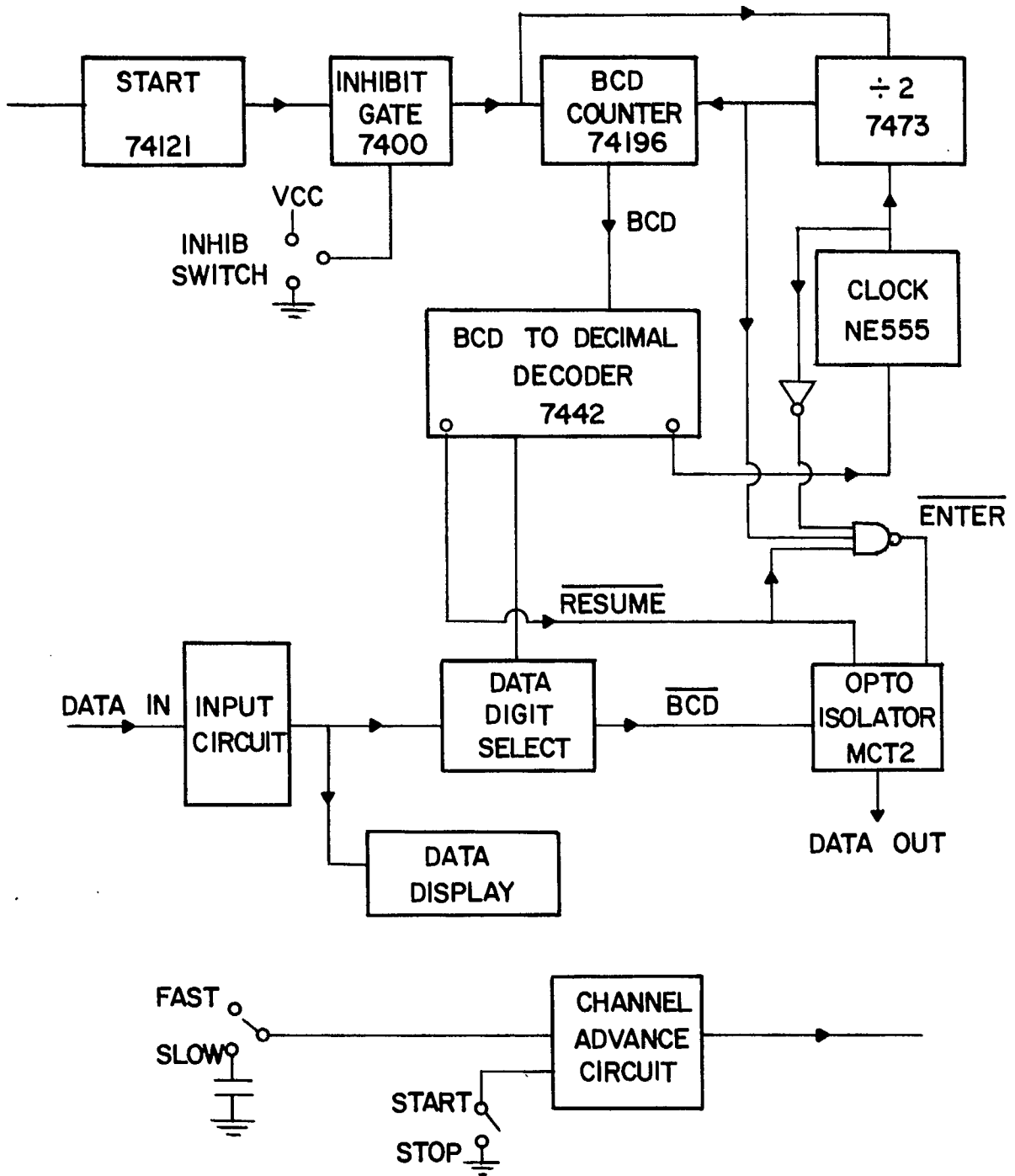
GEA/drs

Figure 1.   Block Diagram of Interface

| | | |
|---|---|---|
| 74121 PIN 1 | | Start command |
| 7442 PIN 1 | | clock control |
| NE555 PIN 3 | | clock |
| 7473 PIN 12 | | sequence pulser |
| 7442 PIN 5 | | Digit sequence 1 M |
| 7410 PIN 8 | | ENTER |
| 7442 PIN 6 | | Digit sequence 2 |
| 7442 PIN 7 | | Digit sequence 3 |
| 7442 PIN 9 | | Digit sequence 4 |
| 7442 PIN 10 | | Digit sequence 5 LS |
| 7442 PIN 11 | | RESUME |
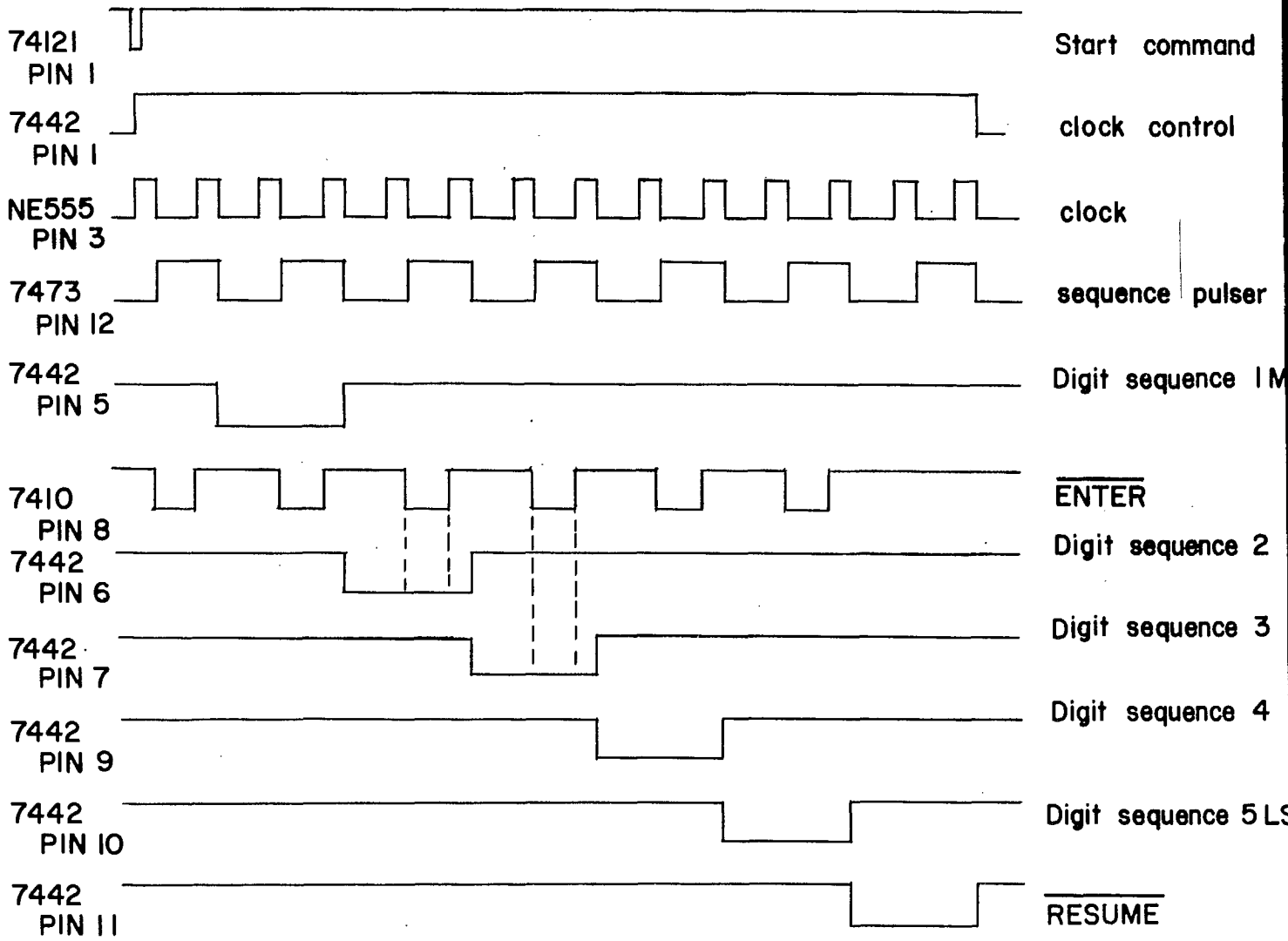
Figure 2. Time Sequence of Interface Pulses

VCC
2NI306

7403 ⑨
K̄I
3
1
2

10K — 26
IK

DIGIT SEQUENCE GATE
AND INPUTS FOR DIGIT 5
(5 CIRCUITS REQUIRED)

VCC
2NI306
K̄2
6
4
5
10K — 25
IK

VCC
2NI306
K̄4
8
9
10
10K — 24
IK

VCC
2NI306
K̄8
11
12
13
10K — 23
IK

⑨

7404 ⑭
4  6  8  10  12
3  5  9  11  13

9  10  11  12  13
EDGE CONNECTOR

⑩ ⑪ ⑫ ⑬

EDGE CONNECTOR

| PIN NO. | FUNCTION | | PIN NO. | FUNCTION |
|---|---|---|---|---|
| 42 | 1 | INPUT | 13 | DIGIT 1 SELECT |
| 41 | 2 | DIGIT 1 | 12 | " 2 " |
| 40 | 4 | BCD | 11 | " 3 " |
| 39 | 8 | | 10 | " 4 " |
| 38 | 1 | INPUT | 9 | " 5 " |
| 37 | 2 | DIGIT 2 | | |
| 36 | 4 | BCD | | |
| 35 | 8 | | 5 | K̄I |
| 34 | 1 | INPUT | 4 | K̄2 |
| 33 | 2 | DIGIT 3 | 3 | K̄4 |
| 32 | 4 | | 2 | K̄8 |
| 31 | 8 | | | |
| 30 | 1 | INPUT | | |
| 29 | 2 | DIGIT 4 | | |
| 28 | 4 | | | |
| 27 | 8 | | | |
| 26 | 1 | INPUT | | |
| 25 | 2 | DIGIT 5 | | |
| 24 | 4 | | | |
| 23 | 8 | | | |

TO SEQUENCE BOARD

Figure 3.  Level Converter Board Circuit

MCT 2 INPUTS TO EDGE CONNECT 8 LEVEL PIN 2, 4 LEVEL PIN 3, 2 LEVEL PIN 4, I LEVEL PIN 5

MCT 2 OUTPUTS TO EDGE CONNECTOR $\overline{K8}$ PIN 16, $\overline{K4}$ PIN 17,

$\overline{K2}$ PIN 18, $\overline{KI}$ PIN 19,

VDD PIN 22

Figure 4. Sequence Generator Board Circuit
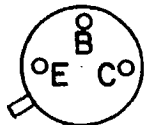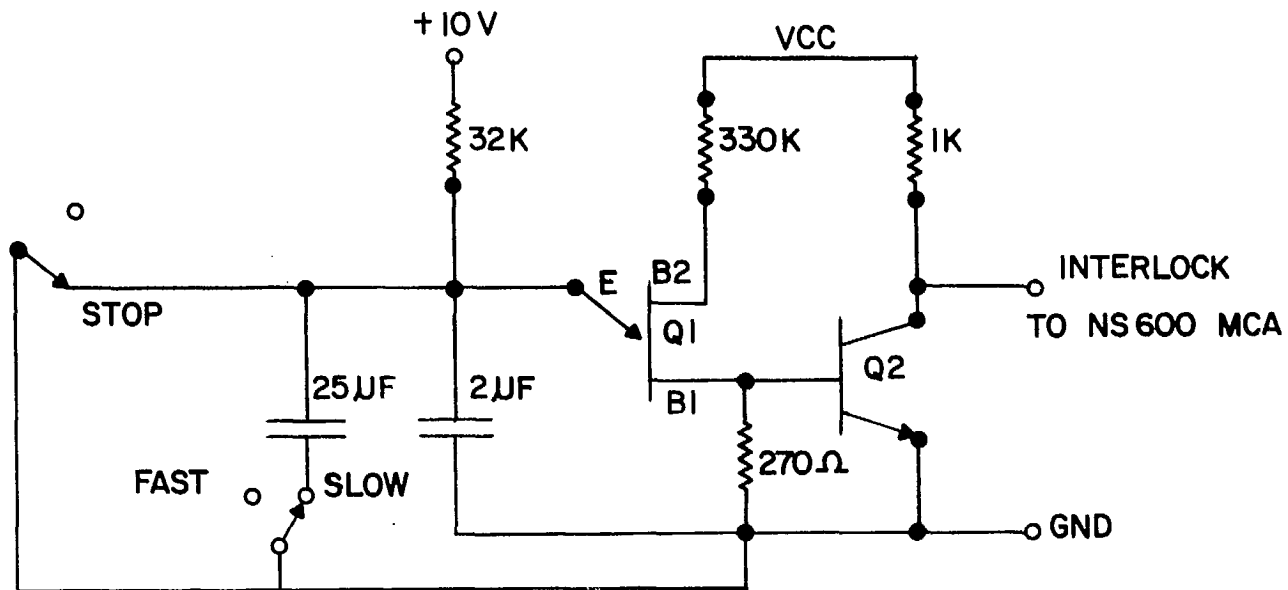
Figure 5.   Channel Advance Control Circuit

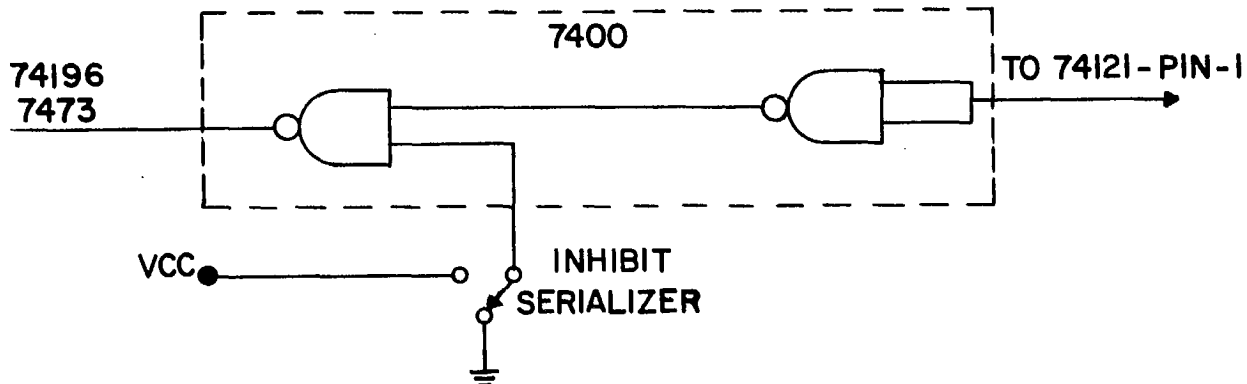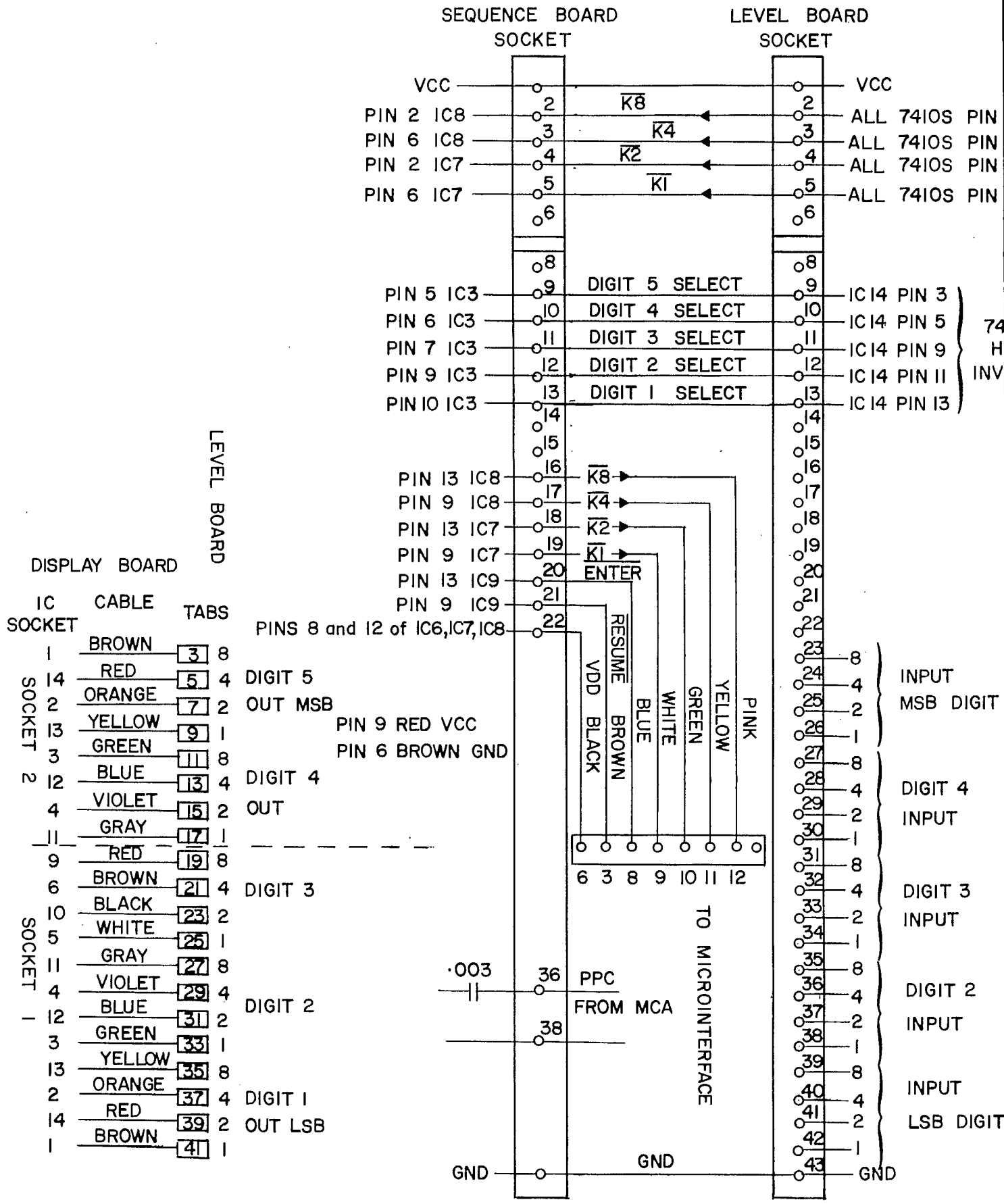## DATA  SEQUENCER  INHIBIT  CIRCUIT



Figure 6.   Data Sequencer Inhibit Circuit

Figure 7. Wiring Diagram for Interface