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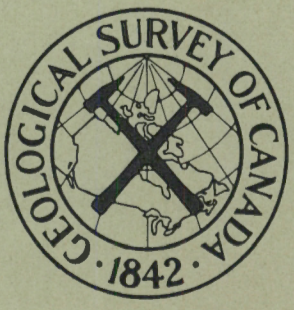

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DEPARTMENT OF ENERGY,
MINES AND RESOURCES

PAPER 70-59

A MINIATURIZED DIGITAL DATA ACQUISITION SYSTEM FOR HIGH RESOLUTION MAGNETOMETER SURVEYING

P. Sawatzky

Price, $2.00

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ABSTRACT

The elaborate procedure required to design a compact digital system suitable for use in relatively small aircraft is described. The system should be useful for agencies and firms who wish to carry out reconnaissance aeromagnetic surveys using digital recording techniques.

A MINIATURIZED DIGITAL DATA ACQUISITION SYSTEM FOR HIGH RESOLUTION MAGNETOMETER SURVEYING

INTRODUCTION

Shortly after the second world war the fluxgate magnetometer made it possible to conduct airborne geological reconnaissance surveys. An accuracy of $\pm$ 1 gamma was considered to be extremely good at that time. Since then, efforts to improve upon this, both by private industry and government agencies has led to the development of proton precession magnetometers, overhouser magnetometers, and the optical pumping varieties such as rubidium, cesium and helium magnetometers. The last named, having the greatest sensitivity, are capable of measuring a thousandth part of a gamma quite accurately.

This increased sensitivity in the art of measuring the magnetic field intensity requires much more accurate navigation equipment to aid in determining when and where each reading is taken. Because of the ability to differentiate between extremely small changes in magnetic field, there is also the requirement that the data sampling rate should be increased so as not to miss the small changes and variations in the earth's magnetic field. All this results in a vast increase in the data that have to be recorded, and later processed.

Computers can be used to speed up data processing and reduce the repetitive aspect of compilation. This however poses the problem of converting the data into digital form, using a format that will be most acceptable in the computer industry. There are several approaches to this problem, but at present it appears as though digitizing and recording the survey data in real time is the best. This does have some drawbacks in that it requires a rather drastic increase in the amount of equipment that must be carried in the survey aircraft which can increase the weight of the survey system several times if the equipment used is that which is readily available on the market.

In the past this has meant that a rather large aircraft was required to accommodate a system which was capable of recording all the essential data, transformed into digital form, on magnetic tape. This was because the equipment required was primarily designed for laboratory use where space and weight were not generally important factors. The size and shape of an instrument was frequently dictated only by what the competition could produce. There has therefore been a need to design equipment capable of performing

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Author's address: Geological Survey of Canada,
601 Booth Street,
Ottawa, Ontario.

all the required functions but reducing the size and weight so that a relatively small twin-engined aircraft, such as an Aero Commander or a Beechcraft Queen Air, could be used.

Figure 1 shows in block diagram form what is required in a Digital Data Acquisition system that is capable of recording the information from sixteen data sources. As the diagram indicates, a considerable number of the necessary components have been reduced in terms of size, weight and power requirements by the extensive use of micrologic in the design. The units that have been miniaturized in this manner are the following:

1. Digital Clock (1)
2. Master Recording Control (1)
3. Interface Gates (16) and Level Converters (3)
4. Shift Registers (3)
5. Tape Monitor Shift Register Control (1)
6. Digital to Analog Converters (2)
7. Digital Volt Meter (1)
8. Mixer and Low Pass Filters (2)
9. Phase Lock Tracking Filters (2)
10. High Speed Counters (3)
11. Shaft Position Encoders (2)

Figures 2, 3 and 4 show front, rear and top views of the digital system that incorporates in one chassis all these components. The complete chassis fits a standard nineteen-inch rack, and weighs about fifty pounds. It consists of three subchassis which are hinged at the back, permitting access to any card for ease of servicing while in flight, or on the ground. The subchassis have been designated A, B and C from left to right. The cards in each subchassis are numbered front to back A 1-20, B 1-24 and C 1-24 respectively. Figure 5 shows the required connections between these digital chassis.

The design of the above units was based upon relatively inexpensive components wherever possible. The micrologic modules used were off-the-shelf items and were manufactured by Motorola and Fairchild. Other types could have been used, but these were both relatively economical, and readily available at the time when this project began in the fall of 1966. All the transistors used in the micrologic modules are of the NPN variety. A one "1" is defined as being positive, and a zero "0" as being zero volts. Thus a transistor amplifier inverter, used in this system, when turned off, will have close to Vcc, the supply voltage, at the collector. This is known as the "1" state at the output. If the amplifier is turned on hard, that is, making the base positive with respect to the emitter, the transistor will conduct hard, and the collector voltage will be very nearly zero volts, or the "0" state.

The symbols used in the circuitry may not conform completely with the practices of some draughtsmen. They have been modified somewhat to make it as easy as possible to draw these schematics. An explanation of the most common symbols and logic functions is given in Figure 6. The 914 type of module has been used extensively because it is the most versatile of the lot. As Figure 6 indicates it can be used in many different configurations, merely by adding a few external components.

The Digital Clock

Anyone familiar with magnetic surveying knows that the diurnal magnetic field variations must be taken into account if absolute accuracy is required when the data is being processed. This can be done by recording the time accurately along with the survey and the ground station data. Care must be taken to synchronize the clocks in the survey vehicle and the ground station precisely to a common standard such as that being broadcast by CHU or WWV.

The accuracy of the clock and other timing circuits will depend directly upon the accuracy of the 1 MHz signal source. As the block diagram, Figure 1 indicates this system uses the 1 MHz output from the frequency synthesizer. If this unit is kept turned on continuously, it has a stability of $\pm 2 \times 10^{-9}$ over a 24 hour period. Thus if the error were all in one direction it would require about three years for the clock to accumulate an error of 2 microseconds.

The logic used in this clock is the familiar 8, 4, 2, 1 code. Table I shows how this code can be used to define any number between zero and fifteen. The divide by ten modules (958), used extensively in this design are composed of four flip-flop circuits inside a TO-5 can. They are capable of counting to sixteen, but internal circuitry permits only ten numbers to be defined, namely zero to nine as shown in Table I.

The clock can provide the following outputs:

1. A visual, six-numeral display.
2. A coded time output, suitable to operate a side marker pen of an analog strip chart recorder.
3. A digital output suitable for recording on magnetic tape and also to code a set of miniature lights in the data chamber of a survey camera.
4. Pulses that occur at regular intervals that can be used to operate other equipment at precisely timed intervals, such as cameras, counters, magnetic tape recorders etc.

The visual display consists of six miniature nixie tubes. Figure 7 shows that each nixie tube is controlled by a decoding matrix module (960). The binary coded information coming from the 958 modules is decoded by the circuitry contained by the 960, and turns on the appropriate number inside the nixie tube. The 958 modules could have been connected directly to the 960 modules, however to provide sufficient drive to permit the taking out of this coded information for recording purposes, the 927 modules were inserted to act as buffers. By having two in series in each line, the proper polarity is again restored to operate the 960 modules.

Figure 8 shows the schematic of the control sequence required to produce a coded trace of the time on a strip chart recorder. The clock is sampled at the even two-minute intervals. The bottom trace of Figure 9 shows how this trace should appear on the record. The rest of Figure 9 shows the pulse sequence that is required to achieve this. The fact that this is made to occur automatically at two-minute intervals somewhat simplifies the shift register requirements since the information from the "seconds" will always be zero at these times. Therefore the coded information for only four numbers need be provided and stored in this shift register. Normally four numbers would require sixteen binary bits to define them, but the tens of

hours can only be a one or a two, which can be defined with two binary bits. The required number of memory elements for the time code shift register, Figure 33, is only fourteen.

The time code is transferred into the shift register in parallel and shifted out serially. Only the last memory element in the shift register, 926-14, Figure 33A, need be sampled every four seconds. If a "1" is present, the recorder pen is deflected for two seconds, if a "0" is present, only a momentary deflection of the recorder pen occurs. The information contained in the shift register is next shifted down one step by applying a short pulse to 914-17 on the shift register card A4. This causes the information stored in the memory units 926-1 to 926-14 to move down to the next lower module. It also causes a zero to be entered into the topmost memory element in the chain. Thus the information stored in 926-13 has been transferred into 926-14, and this module is again sampled for a "1" or a "0". Thus, after fourteen, four-second intervals, the complete number will have been transferred to the chart. After this only zeros will be recorded until the long dash occurs which lasts for ten seconds. The end of this denotes the start of the next two-minute time interval.

Each number displayed by the nixies is also available in an 8421 code. This may be recorded on magnetic tape, or printed on paper tape. The coded information has been boosted to a higher level of about plus ten volts, because most printers and magnetic tape recorders require this level. The level conversion takes place on card B20, Figures 12 and 13. This information may also be transferred to the survey film by coding a set of miniature light bulbs, the size of rice kernels, installed in the data chamber of a survey camera. The time information provides positive identification of every photograph, and also relates it to the survey data as recorded on magnetic tape, the strip chart recorder and the printer tape.

The clock also provides pulses that occur at regular intervals which may be used to operate other equipment such as cameras, counters, digital voltmeters etc. These pulses originate in the count down chain preceding module 958-9 of Figure 7. They have been isolated and shaped by means of one-shot multi-vibrators.

The design of the clock was slightly complicated by the fact that several of the divide-by-ten modules have to be reset to the zero state before they have reached this state on their own account. Thus in Figure 7, the tens of seconds module 958-10 must be reset to zero on the sixtieth "second" pulse arriving at module 958-9. The tens of minutes module 958-12 must be reset to zero on the sixtieth "minute" pulse arriving at module 958-11. The units hours module 958-13 must be permitted to reset to zero naturally at the tenth and twentieth hours, but must reset to zero along with the tens of hours module 958-14 when the 86,400th "second" pulse enters module 958-9, because at midnight the display must be 00-00-00; zero hours, zero minutes and zero seconds. These reset pulses are produced at the correct intervals by the one shot multivibrators 914-14, 914-15 and 927-12, which are triggered by the "NAND" gates 927-4, 927-8 and 927-12.

Special circuitry is required to enable the operator to synchronize this clock with the time signals being received by the WWV receiver. Figure 7 shows this circuit which is composed of the following modules, 923-1 to 4, 958-3, one half of 914-2 and modules 914-3 to 6 inclusive. The output from 958-1 which is 100,000 pulses per second (PPS) is fed to 923-1. At pin 5 of 923-2 the output frequency will be 25,000 PPS which is further divided by 2, 3 and 4. This produces the following frequencies which are made available at

the input of 958-4; 25,000 PPS, 12,500 PPS, 8,333 1/3 PPS and 6,250 PPS. In addition there are 10,000 PPS available via the rest position of SWA-3.

These frequencies are selected by means of SWA-3, which is spring loaded, and returns to the centre position when the pressure is released, and SWA-2. By placing SWA-2 in the ADVANCE position, 25,000 PPS are available at the terminal marked FAST of SWA-3 and 12,500 PPS are available at the terminal marked SLOW of SWA-3. Both of these frequencies are higher than the 10,000 PPS available in the rest position of SWA-3. Thus by accepting 25,000 or 12,000 PPS at the input of 958-4, the pulses from 914-10 will occur at a faster rate than those coming from the WWV receiver. The "second" pulses can thus be made to catch up to those coming from the receiver.

If it is found desirable, the switch SWA-2 can be placed in the RETARD position. The following frequencies are then available at SWA-3, 8,333 1/3 PPS at the terminal marked FAST, 10,000 PPS at the centre terminal, and 6,250 at the terminal marked SLOW. By accepting either 8,333 1/3 or 6,250 PPS at the input of 958-4, the output of 914-10 will be slower than those coming from the WWV receiver. In this case the pulses from the receiver will catch up to the "second" pulses coming from the clock.

Therefore by using either method, the one second pulses coming from the clock can be brought into synchronism with those being transmitted by either CHU or WWV. Once they are in synchronism the pressure on SWA-3 should be released. Normal operation of the count down chain up to module 958-8 is then resumed. Note that it is not enough to bring the "second" pulses into alignment, the minutes and hours must also be correctly set and synchronized.

To accomplish correct synchronization it is necessary to first preselect a time when it is desirable that the clock should start. This is done by setting SWA-1 to the SET TIME OF DAY position, Figure 7. This permits the selection of higher frequency pulses than the normal, one pulse per second to enter the display section of the clock by means of switches SWA-4 to SWA-8.

Let us assume that the required time when the clock is to start is to be 10-05-00 (ten hours, five minutes, zero seconds), and that it is 10-00-00 at present. The visual display is then set to the desired starting time by means of switches SWA-4 to SWA-8. As the display approaches the desired value the lower frequencies should be used. After the display has been set to 10-05-00 it is necessary that the "second" pulses that are to activate the display section be synchronized with those transmitted by WWV or CHU.

To accomplish this a dual beam oscilloscope is most useful. To use this instrument, connect the input of channel A to the 1 PPS output of the clock, JA-8, Figure 3. Trigger the oscilloscope from this same point. Next attach the channel B input of the oscilloscope to the earphone jack of the WWV or CHU receiver. With the oscilloscope properly adjusted the pulses from the clock and the receiver should both be visible on the screen. To bring the two pulses into synchronism, the clock pulses may be either advanced or retarded with respect to the radio receiver pulses by means of SWA-2 and SWA-3. The rate of advancing or retarding may be selected with SWA-3. After a little practice, this synchronization procedure may be completed in a minute or so. After the clock has been set to the desired starting time, and the one second pulses have been synchronized with WWV or CHU, all that

remains to be done is to flip the switch SWA-1 to the OPERATE position within a period of one second from the time that the received signal indicates 10-05-00.

If no oscilloscope is available, a small light bulb may be used to synchronize the one-second pulses. This may be done by connecting the small light bulb across the 914-10 module. This can be done by connecting the bulb between JA-8 and Vcc. By listening to the "second" tick coming from the receiver and watching the flashing of the light, the pulses may be synchronized.

Figures 10 and 11 give the card layout and the inter-card wiring for the digital clock. Figure 14 shows how the digital time code may be connected into the data chamber of the survey camera. By recording the time on the survey film, the position data can be related precisely to the other records. In addition, the time may also be used to number the exposed frames.

The Master Recorder Control

The master recorder control consists of cards A5-10 inclusive. This is the heart of the digital recording system, and as the block diagram Figure 1 indicates, it performs several functions. These, and the requirements for each, are listed below.

1. Rate of Scan

a) The rate at which the gates are to be scanned should be variable, depending upon the ground speed of the survey aircraft.
b) It should be possible to select the source of the pulses that regulate the scanning rate.

2. Data Block Length

a) The data blocks should be of equal length for any one project.
b) The data block should always begin with the information stored in, say gate 0, and end with the information obtained from gate 15.
c) The inter-record gap should not occur except after the end of a complete scan of all sixteen gates, and only after all the information has been recorded.
d) It should be possible to vary the data block length easily if required and retain the above conditions.

3. Camera Firing Rate

a) The rate at which the camera is fired should be easily controlled and variable.
b) The camera firing rate should be synchronized with the scanning rate.
c) Provision must be made so that the camera may be fired manually if required.

4. Recording Rate

a) The recording rate pulses should be variable.
b) It should be possible to select various sources for the pulses that determine the recording rate.

5. Gate Selection

a) It should be possible to select which data sources shall be accepted and recorded.
b) It should be possible to determine how often each data source is accepted for recording purposes in each data block.

6. Digital to Analog Converters and Printer Control Pulses

a) The Master Recorder Control should provide the pulses required to operate the Digital to Analog converters and printer.
b) These pulses should be synchronized so as to occur at the proper time.
c) It should be possible to select the data that is to be monitored.

To explain the operation of this section of the digital system consider Card A5, Figure 15. This card can accept pulses from two sources, the doppler radar and the digital clock. Figure 15 shows SWA-10 in the position that puts 100 PPS into module 958-1. This is reduced to 20 PPS by the first three modules 958-1, 914-8 and 914-3. These pulses can be divided further by means of the next four modules, 958-2, 960-1, 914-9 and 914-5. Since the 960-1 module is a decoding matrix it is possible to use it, together with a switch, to select the rate at which the 958-2 module is reset to zero. This in turn determines the rate at which all of the gates are being scanned. The switch SWA-30A is shown in a position where every eighth pulse will reset 958-2 to zero. Therefore the rate of scan pulses will occur at $1/(20/8) = 0.4$ second intervals. The selectable intervals range from 0.15 to 0.50 second for the condition where SWA-10 is in the position shown.

If the rate of scan pulses were to occur at two per second and the aircraft ground speed were 180 miles per hour thus the distance travelled per sample of all the gates would be $\frac{5280 \times 180}{2 \times 60 \times 60} = 132$ feet. This is equal to $\frac{5280}{132} = 40$ samples per mile. It is possible, by means of SWA-10 to switch to the position where pulses originating in the doppler radar, which are linked to distance gone, could be used to trigger the rate of scan generator. To maintain a sampling rate of 40 per mile the minimum pulse rate required would be 600 pulses per mile. The fastest pulse rate that could be accommodated yet still result in 40 samples per mile would be 2,000 pulses per mile.

The rate of scan pulses are also used to determine the data block length. The block length is determined by the setting of SWA-35A. Figure 15 shows it set to produce an Inter Record Gap (IRG) pulse after all the gates have been scanned twice. The shortest data block length is one scan, the longest requires all the gates to be scanned 256 times. Provision had to be made for the IRG pulse to occur after all the information from the last gate had been recorded. This was accomplished by the small circuit located on card A 10, shown on the bottom left corner of Figure 15. This circuit inhibits the One Shot (OS) multivibrator 914-2 from producing an IRG pulse until the End of Gate (EOG) pulse has set the Flip Flop (FF) multivibrator 914-14 and the $\overline{b\ 15}$ pulse has set FF, 914-13. This permits the next Recording Rate (RR) pulse to pass through the Nand gate 914-12 and also to reset the FFs, 914-13 and 914-14 which effectively closes the Nand gate again. The pulse that triggers the OS, 914-2 causes the IRG pulse to be produced. The IRG pulse resets the block-length counter 923-1 to 923-9 back to zero. It sets the Test FFs on Gate cards 0 and 1, and also gives the signal to the magnetic tape recorder to produce an inter-record gap, which terminates a data block.

The rate at which the survey camera exposes film is also determined on these cards, A5 and A10. For this purpose the rate of scan pulses are fed into a divider circuit capable of dividing the incoming frequency from 1 to 10. The modules performing this function are 958-4, 960-3, of Figure 15 and 914-7, 914-8, 914-10 and 914-11 of Figure 15A. By using the rate of scan pulses the camera firing rate will always be synchronized with the rate at which data are gathered, no matter whether the rate of scan pulses originate in the clock or in the doppler radar unit. Thus to ensure adequate overlap at all times the camera firing rate can be varied to suit the ground speed and height at which the aircraft is flying. With the switches set as shown in Figure 15 the rate of scan pulses occur every 0.40 second, the camera would then receive a pulse once every 0.40 x 8 = 3.20 seconds.

For survey purposes it frequently is desirable to expose extra frames, for instance when the aircraft is exactly above some readily identifiable feature such as a stream, a road, a lakeshore, a point of land etc. These extra frames should also be identifiable. To meet these conditions an extra module was added to the camera firing circuitry, namely FF, 914-12, Figure 15A which is located on card A10. The momentary contact switch is located at the end of an RG58U cable and connected to the circuit via JA-15, so that the navigator may operate it. The momentary contact closure of the switch SWA-38 sets FF, 914-12 causing pin 7 to go to "0" and pin 6 to go positive. This causes the output of 914-7 of Figure 15A to go positive, which in turn triggers the OS, 914-8, causing it to produce a camera firing pulse. The inverted trailing edge of this pulse resets FF, 914-12. The purpose of FF, 914-12 is to cause one of the lamps, namely the 8 of the tens of seconds group which normally would not come on in the camera data chamber to light thus marking the frame (see Figs. 12, 13 and 14).

The Recording Rate (RR) pulses are generated in modules 958-3, 960-2, 914-4 and 914-6 of card A 5, Figure 15, 1,000 PPS enter the module 958-3. This set of modules form another variable divider circuit. By means of SWA-31A, the repetition rate may be selected to produce from 100 to 500 PPS. With SWA-31A set as shown it would produce 125 PPS. RR pulses are also produced by the Free Running (FR) multivibrator 914-5, Figure 16. By setting SWA-31A Figures 15 and 21, to position 1, these pulses would be used instead of those coming from card A 5. These would be fed back to card A 6 via SWA-30A and SWA-30B. For test purposes the OSs, 914-3 and 914-4 Figure 16 may be used by means of SWA-30A and SWA-30B. The recording sequence may be run through by first pressing SWA-10 which simulates the rate of scan pulse. Manual RR pulses may be produced by pushing SWA-20. By using the above switches the recording sequence may be checked for correct operation.

Figure 16 shows the magnetic tape recorder pulse sequence timer which consists of counters A and B and associated control circuitry. The functions of this card (A 6) are intimately related to those of cards A 7, A 8 and A 9, which produce the Pulse to Unit, Test and Ignore pulses. An understanding of what happens on A 6 will require reference to what is happening on the last three cards as well. They affect the operation of card A 6, whether it will produce pulses to operate the digital magnetic tape recorder or not. The functions of this card (A 6) probably are best explained by referring to Figures 1, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21 and 22, with special emphasis on Figure 22 which shows the correct pulse sequence when gates 0,

3 and 4 have been selected to present data to the shift register for recording purposes. Gates 1, 2, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14 and 15 have been blocked as shown by Figures 18, 19 and 20.

Referring to Figure 16, assume that a rate of scan pulse has just arrived from card A 5, Figure 15. This will set FF, 914-10, provided that it does not occur while the inter-record gap is being produced by the magnetic tape recorder. It will also reset the counters A and B to the zero state. Counter A being module 958-1, the counter B being modules 923-1, to 923-4. Setting 914-10 opens gate 914-13 (output pin 7) which permits RR pulses which have been shaped by the OS, 914-6 to set FF, 914-11, provided the $\overline{\text{Test}}$ line is negative. This is determined by the position of the gate selector switches and the state of the FF module on the gate cards. If we are starting a new data block, gate 0 will have its Test FF module in the set state because the pulse that does so is the IRG pulse. Setting FF, 914-11 opens gate 914-13 (output pin 6). A RR pulse can now enter counter A, producing the (0001) condition in the 958-1 module, and the OS, 914-15 module, producing a delayed pulse that enters the counter A state into the buffer memory, 959-1 module. It also successively triggers OSs 914-17 and 914-18. Table II shows that this is the correct state for gate 914-21 to be in for a $\overline{\text{Transfer}}$ pulse to be passed, which is used to enter data into the Shift Register (SR) via the interface gate 0, Figures 1, 12, 13 and 21. The same pulse, slightly delayed, that produces the $\overline{\text{Transfer}}$ pulse also triggers the OS, 914-18, which in turn produces a $\overline{\text{Strobe}}$ pulse which is used to initiate the recording sequence in the magnetic tape recorder. To prevent recording errors, this pulse is delayed slightly so as to give the data which has been entered into the SR to "Settle down" before the first four bits are recorded on magnetic tape.

During this interval pin 7 of the gate, 914-22, was positive; therefore the pulse producing the $\overline{\text{Transfer}}$ pulse was not able to produce a $\overline{\text{Shift}}$ pulse (see Table II for the states of A 1, A 2, A 3, and A 4). RR pulse No. 2 will enter counter A and the 0010 state will be entered into the buffer memory. This new state will cause pin 7 of gate 914-22 to go negative before the delayed pulse arrives at pin 5 of 914-22. This permits a $\overline{\text{Shift}}$ but not a $\overline{\text{Transfer}}$ pulse to be generated. The $\overline{\text{Shift}}$ pulse causes the four bits which already have been recorded to be dumped from the SR and the next four to be moved into position. The $\overline{\text{Strobe}}$ pulse which follows a fraction of a microsecond later again causes them to be recorded on magnetic tape.

Each interface gate permits 20 binary bits to be loaded into the SR in parallel. Thus after one $\overline{\text{Transfer}}$ pulse and four $\overline{\text{Shift}}$ pulses these 20 binary bits will have been recorded. In order that the output from each interface gate may be tagged, the state of the B counter is recorded after the last group of four bits comprising the survey data has been recorded. This requires a sixth RR pulse. As Table II indicates, this opens the gate 914-20 and lets an End of Gate (EOG) pulse to be formed. The EOG pulse initiates the B counter so that the (0001) state will be stored in modules 923-1 to 4 (see Table III).

This EOG pulse is also used to reset the A counter and the FF 914-11 which closes gate 914-13 (output pin 6). The next RR pulse therefore will attempt to set FF 914-11 but can do so only when the Test line is negative. Figures 18, 19, 20 and 22 indicate that this gate has not been selected. Because the 914-11 FF cannot be set, the output of the amplifier inverter 900-2 will be negative. Figure 18 shows that this is a requirement to provide for the case where an interface gate has been selected but the data is not to be

recorded except when the gate FF has been set. Gate "0" will present such a condition at least once in each block of data because the pulse that sets the gate "0" FF is the IRG pulse.

With the Gate selector switch SWA-12 as shown in Figures 18, 19 and 20, the gate 914-2 of Figure 18 is able to pass an RR pulse which has been shaped and amplified by 914-25 and 900-1. This pulse can be traced through the various Nand and Nor gates, emerging finally as an Ignore pulse from 914-24. This is fed back to card A 6, Figure 16, module 914-19 where it produces an EOG pulse. This again performs the functions described for this pulse previously.

The "B" counter will now contain a (0010) 2. The third RR pulse will again test to see if FF, 914-11 can be $\overline{\text{set}}$. As indicated by Figures 18, 19 and 20, this is not possible since the Test line will be positive. Because of this another Ignore pulse will be generated which in turn will again produce an EOG pulse. This will cause the B counter to contain a (0011) 3. As shown by Figures 18, 19, 20 and 22 this gate is to be sampled. Therefore the sequence of events will be repeated as described for Gate "0". All the interface gates will be tested in this manner. The recording sequence will cease after Gate "15" has been dealt with which completes one scan of the Gates "0" to "15". The recording sequence will be initiated again by the next rate of scan pulse, which as noted previously will occur every 0.40 second with the control switches set as shown in Figures 15 and 21.

Card A 7, Figure 17, contains the Pulse to Unit (PTU) control. It takes the code generated by the B counter and decodes it into sixteen identities from 0 to 15 and produces b 0 to b 15 and $\overline{\text{b 0}}$ to $\overline{\text{b 15}}$ pulses that are used to select and inhibit the Gates "0" to 15 by means of the switches shown in Figures 18, 19 and 20. These pulses are also used to control the $\overline{\text{Test}}$ and Ignore generator circuits.

On the bottom right hand corner of Figure 17 there is a small circuit composed of modules 914-17 to 19 and the PTU selector switches SWA-32A, SWA-32B, SWA-33A and SWA-33B, Figure 20, which produces a pulse labelled $\overline{\text{D/A READ}}$. This permits the monitoring of any one of the Gates "0" to "15" by commanding the Digital to Analog Converter and the Printer to display the contents of the shift register immediately after the information has been entered into it by the $\overline{\text{Transfer}}$ pulse. Thus by means of the PTU selector switches the data passing through any one of the sixteen gates may be monitored by means of the printout system or on strip chart recorders. This can be extremely useful when checking the system or trouble shooting. To identify the gate being monitored on the printer, a code is generated by a diode matrix shown on Figure 21, and switches SWA-33A and SWA-33B. Figures 23, 24, 25 and 26 show the card layout, the intercard wiring and the connections required between the digital system and the magnetic tape recorder.

The Interface Gate Cards

The function of the Interface Gate Cards is to permit data from the various sources to reach the Shift Register Stage thence to be transferred to the magnetic tape recorder. Figure 27 contains information useful when checking the magnetic tape and also the digital system. The first five columns list the interface gates in sequence, show where they are located, what the data source for each one is and how often each is recorded. Columns six

and seven show how the gate identifiers should look on the magnetic tape when a bit in the "B" column is used as an identifier. Columns eight and nine contain similar information for the case where a bit in the A column of the magnetic tape is used. The last two columns indicate how the survey data should look when recorded using the IBM code.

Figure 28C contains a schematic or logic diagram of the interface gate of which there are sixteen in this system. The output side of all these gate cards "0" to "15" enter the shift register (Fig. 12). The diodes at the output of each of the output terminals provide isolation between the various cards and prevent interference. All the outputs will be low or in the "0" state between transfer pulses because of module 900-1 which holds the gate line positive between pulses. Only one gate card at a time can receive a transfer pulse via the PTU card, Figure 17. Assume that it is required to read gate "0" as already discussed above. To do so the gate selector switch SWA-11 must be set to position 2 as shown in Figure 20. The FF, 914-11, Figure 28C must have been set. Figure 27 indicates that this occurs only once per data block because it is the IRG pulse that performs this function. If an IRG pulse has been received, pin 48 of card A 11 must therefore be positive. This is connected to module 914-1 pin 1 of the Test pulse generator, Figure 19, and module 914-1 pin 2 of the Ignore pulse generator. This inhibits the Ignore pulse generator, but causes the output of the Test pulse generator 914-23 pins 6 and 7 to go negative. This is the condition discussed previously, that is required to enable the data from gate "0" to be transferred and recorded. The trailing edge of the pulse applied to the gate line is applied to the OS, 914-12 Figure 28C. This resets FF, 914-11 and prevents this gate from being sampled again until another pulse comes along to set FF, 914-11 on the gate card.

As noted previously, the digital system is housed in three subchassis A, B and C. Each contains several interface gate cards. Figures 30, 31 and 32 show the intercard wiring of these cards in the three subchassis. In addition, Figure 30 shows the thumb wheel switches, required to provide the coded information for Gates "0" and "1" (also see Fig. 27). Figure 32 also contains some additional information besides the wiring of the gate cards in subchassis C, namely the wiring information for the Phase Lock Tracking Filter cards C 14 and C 16 to be discussed later. Figure 29 shows the card layout of the three types of circuits shown in Figure 28.

The Level Converters

Level converter cards are used in this system because of the requirements of the magnetic Tape recorder and the Hewlett Packard Digital to analog converter and Printer. Both of these units require signal input levels that vary by at least 10 volts. In this case, the card changes the micrologic signal level (0 to +4 volts) to 0 volts and +12 volts. Two types of cards are used, Figure 28 shows both of them. The one on the left, Figure 28A has a double inversion feature that provides the proper signal polarity as well as signal level for monitoring the output of the digital clock output on the printer. The majority of transistors used in this digital system are located on these level converter cards.

There are two sets of twenty miniature lights on the front panel of the B chassis, Figure 2. Each one of the lights is in series with a resistor,

together forming the collector loads for the transistors. The resistor value was chosen to provide the correct voltage across the bulb. The bulb glows when the collector is low, therefore indicating the "0" state in this case, and not the "1" state.

Each group of twenty lights is subdivided into five groups of four lights. From Figures 12 and 13 it will be seen that each light will indicate the state of one of the shift register memory modules. This visual indication is an aid in checking the operation of the digital system. During normal operation the rate at which data pass through the shift register is too fast for the human eye to discriminate, but when the system is put into the Test or check mode as described earlier, where manual pulses operate the system, then these lights can indicate to the human eye the correct operation of the system. These lights therefore have no application except to help in checking out the digital system. The top group of twenty lights aids in checking out the data acquisition system before the data are recorded on the magnetic tape. The lower group of twenty lights has been installed to check the data coming back from the magnetic tape recorder (Figs. 12, 13 and 14).

There is a third set of lights located in the survey camera data chamber which have already been mentioned (see the discussion on the Digital Clock). They are also operated by a level converter card, in this case B20, which provides a double inversion, thus providing the proper polarity to operate the lights as well as the printer.

The Shift Registers

Two types of shift registers are used in this digital system, Figures 33, 34 and 35. These are the time code shift register and the data shift register. Both types use the 926 micrologic modules as the memory elements. The time code shift register which is shown on the left of Figure 33 has been designed to accept fourteen bits in parallel by means of a $\overline{\text{Transfer}}$ pulse. The information thus entered is then moved out serially, one bit at a time, by means of $\overline{\text{Shift}}$ pulses. The state of the last memory module 926-14 being sampled once for each $\overline{\text{Shift}}$ pulse.

The "Set" and "Clear" input points of module 926-1 are connected to zero volts and Vcc respectively. This ensures that the shift register will be progressively loaded with zeros from the top as the binary coded time information is being shifted downward. Therefore after the time code has been recorded on the chart, which requires 14 x 4 = 56 seconds, the marker pen will be deflected only long enough to cause a sharply defined blip which can be related to the time, because they occur at four-second intervals, and to the survey data that are being recorded. (For a further discussion of the time code shift register and its operation see "The Digital Clock").

The data shift register is designed to accommodate twenty binary bits at one time. The information is entered in parallel via the interface gates "0" to "15", Figures 12 and 13. There are two complete data shift registers, the direct monitor shift register and the tape monitor shift register. Each one consists of two identical cards, interconnected as shown on the right of Figure 34.

Immediately after the direct monitor shift register has been loaded with new information its contents may be checked for accuracy. There are three methods available to the operator to accomplish this. As noted under

the heading of "Level Converters" there is a set of small lights located on the front panel of the B chassis that may be used for this purpose (Fig. 14B). This can only be done when the recording rate pulses are produced manually as discussed under the heading of "Master Recorder Control". The second method is to use the digital to analog converter, which, as the name implies, converts the coded information into an analog voltage suitable for recording on a strip chart recorder (Fig. 38). The third method of checking is to pass this information on to an external digital to analog converter and printer (Figs. 12 and 13). As these two figures indicate, the printer output will contain three bits of information, the time, the number of the gate via which the data reached the shift register, and the contents of the shift register all in numerical form. This checking process does not interfere with the operation of the magnetic tape recorder. The second and third methods may be employed while the system is in operation. The information thus obtained can be very useful as a permanent record or for comparing it to that which is known to exist prior to being fed into the digital system.

The data shift register is wired in such a way that each $\overline{\text{Shift}}$ pulse moves four bits of information at a time into the next lower four memory units. It requires one $\overline{\text{Transfer}}$ and four $\overline{\text{Shift}}$ pulses to move the whole twenty bit number into the recording position, a fifth $\overline{\text{Shift}}$ pulse moves the "B" counter state into the recording position. This last bit of information tags each five-number group and makes it possible to monitor the survey data that have been recorded on the magnetic tape while recording is in process (see Table IV).

The tape monitor shift register is used to reassemble the information coming from the magnetic flux check section of the magnetic tape recorder (Fig. 13). The information enters this shift register in parallel, four bits at a time. After the fifth group has been entered into the tape monitor shift register, the number that was previously in the direct monitor shift register should now be in the latter. The sixth four bit group together with the gate identifier causes a pulse to be produced that samples the information contained in the tape monitor shift register. It may be recorded or printed out in a manner similar to that already discussed for the direct monitor shift register.

After this has happened the four bits comprising the gate number are also entered into the tape monitor shift register. This alters the contents of the shift register but it no longer matters because the numbers that were in the shift register, at the time the sample pulse was generated, have already been recorded. In this manner the pre-selected gate, say gate nine, Table IV, will be recorded every time it occurs in the recording sequence. If gate nine was also being monitored by the direct monitor system, then the two sets of traces may be compared and checked for errors while the survey is in progress. If errors should occur, the system would automatically pinpoint where and when the error occurred because, as described earlier, the chart recorder is marked accurately with a digital time code (see the description of the "Digital Clock"). Figure 35 shows the intercard wiring of the various shift registers in the whole system.

The Tape Monitor Shift Register Control

During the discussion of the "Master Recorder Control" it was noted that the digital to analog converter that is used to check the data contained in the direct monitor shift register, receives its control pulses from card A 7. This is also true for the monitoring system contained in the Hewlett Packard unit when it is used in the direct monitor modes. The digital to analog tape monitor however is controlled from the tape monitor shift register control card, Figures 36, 37 and 38. When the Hewlett Packard digital to analog converter and printer are used to display the information coming from the tape monitor shift register, it too is controlled by this card.

Let us assume that we are monitoring a bit of magnetic tape shown in Table IV. The data numbers recorded on the tape are 9999, and the gate number is also nine, using a bit in the B column to indicate that this is the gate number. The data are taken from the flux check stage of the Kennedy magnetic tape recorder, and presented to the buffer memory module 959-1 (Fig. 36). The recorder also puts out a "flux check complete" signal that is used to trigger several OS units, 914-2, 914-3, 914-5 and 914-6. A pulse is produced by 914-2 and 914-4 (pin 7 output) that enters the information into the buffer memory. The delayed output of 914-3 and 914-5 produce a $\overline{\text{Shift}}$ pulse that enters the latest four bits into the tape monitor shift register. The delay has been introduced to permit the contents of the tape monitor shift register to be checked at the appropriate time before new information is entered. After five "flux check complete" pulses have been received, the whole number will have been assembled in the shift register. The sixth "flux check complete" pulse will pass through gate 914-7 because the signal from the B channel and the signal from the gate number decoder matrix modules 960-2 and 960-1 have opened the gate. This produces a pulse that triggers the tape monitor digital to analog converter and causes it to sample the contents of the tape monitor shift register. As already noted the Hewlett Packard digital to analog converter and printer may also be operated by this pulse.

Figure 36 shows the system monitoring gate "9", but any one of the other gates could have been selected. After the check has been completed, the shift pulse takes over again and moves the latest four bits from the buffer memory unit into the shift register. This action changes the number in the shift register, but as already noted this no longer matters since the part we are monitoring has already been entered into the memory elements of the digital to analog unit.

The Digital to Analog Converters

Digital to analog converters can perform very useful functions when operating a digital recording system. The older more conventional survey systems recorded all of their data on strip chart recorders which presented the operator with a continuous visual check of the system's condition. Whenever equipment trouble occurred it was immediately apparent to the operator. When recording the survey data on magnetic tape this no longer is the case. Some means must therefore be provided to enable the operator to obtain a real time visual check of what is going onto the magnetic tape unless one is prepared to take a chance that everything is functioning properly. This may work well enough in a laboratory where an experiment may be repeated if

necessary, but when conducting a survey this is not always possible and extra precautions are required to ensure correct operation of the system.

Provision has been made in this system to use a commercial digital to analog converter which together with a chart recorder and a printer, can perform this function. However this commercial unit is extremely bulky and to eliminate this drawback, two digital to analog converters were designed and built using micrologic modules (Figs. 38, 39 and 40). As Figure 39 indicates, the digital to analog converter shown on the left monitors the data that are going to be recorded on the magnetic tape and is called the direct digital to analog monitor. The one on the right obtains its information from the magnetic tape recorder and is called the digital to analog tape monitor.

The digital to analog converter consists of only a few modules and a multiple deck switch. With this arrangement it is possible to monitor two adjacent groups of four bits, each group of four representing one numeral. With the switches set as shown in Figures 17, 38 and 39 the 959 modules would obtain the information contained in gate "15", the height above ground (see Fig. 27).

Module 722 B performs the functions of switches that are either open or closed, it and the resistor network to the right of this module produce the analog voltage appropriate to the numbers, in coded form at the input, that is supplied by the 959 modules. Module 959-1 would receive the least significant, 10°, and module 959-2 the information for 10^{1}. The combined output to the recorder would be between:

Position	1	0 -	99
	2	0 -	990
	3	0 -	9,900
	4	0 -	99,000

The direct monitor digital to analog converter output checks the information going to the digital magnetic tape recorder and presents an analog voltage to a recorder. The tape monitor takes the information coming from the digital magnetic tape recorder and presents it a few milliseconds later in a similar analog fashion to another channel of the same chart recorder. If an error has occurred either in the system prior to recording or during read-back, then the traces will show this. The flexibility of the digital to analog monitor units permits a very thorough check of the complete digital system.

The Digital Volt Meter

The present survey system has only two data sources that appear as analog voltages in their original form, namely the output of the radio altimeter and the across track error voltage from the doppler radar. In order that they may be recorded in digital form, a digital voltmeter has been added to the system (Figs. 38, 41 and 42).

The digital voltmeter may be initiated from two points, a switch on the front panel, or a positive going pulse applied to pin 1 of module 914-3 via the multiplexer card. This applies a reset pulse to the binary counter modules 923-2 to 923-10, which in turn causes the voltage ramp, generated by the switching network 722 B-1 and the resistor network, to return to the zero level. This in turn causes the voltage comparators 741-1, 2, 3 and 4 to produce an output signal at gate 914-5 that will go to zero volts. This in turn

permits the OS, 914-1 to operate, thus passing the 1 MHz clock pulses that originate in the frequency synthesizer. A count will then be accumulated in the 923 modules, which in turn will produce a voltage ramp at the output of module 741-1. The increasing amplitude of the voltage ramp is continuously being compared with the input voltage that is to be measured by the modules 741-2 and 3. When the ramp voltage equals that of the voltage to be measured, the voltage comparators cause the output of gate 914-5 to go high. This action produces two results; (1) the 914-1 module is cut off, thus preventing any more pulses from entering the counter section of the system, and (2) the positive step function produces a pulse that triggers the 914-4 OS module. The resulting pulse enters the state of the 923 modules into the buffer memory stages 959-1 to 3, which in turn cause the decoding matrix modules to produce a display in numerical form on the front panel of the B chassis.

The 722-B switching network is capable of handling the output from ten binary counter modules. This would be enough to produce a decimal display of 0 to 99 with two binary bits left over that would be meaningless in themselves. Using an octal numbering system, all the binary bits can be used and the voltage ramp can be extended to include the values from 0 to 1023 which is an improvement of greater than ten. By grouping the digital output into groups of three, an octal output is obtained which permits the use of a standard decimal display, with the exception that the numbers eight and nine will not be activated in this system. The digital code is recorded in groups of four digits, but in this case the 8 of the 8421 code is always a zero state. which permits the regular monitoring system to be applied to this data source.

Because the output appears in the octal system, a count of 1,000 to the base ten will appear as a higher number, in this case 1,750 to the base eight. To change from one to the other is quite simple. To change $1,000_{10}$ to a number to the base eight; divide the higher base number by the base of the lower and keep track of the remainder (see Fig. 42 C). To go from the lower base number to the higher base number, multiply the most significant by the lower base, add the second most significant number to the result and repeat the process (see Fig. 42 D). A conversion table, Table V, octal to decimal integer conversion, is included that permits quick conversion from numbers of one base to another.

The voltage ramp height available at the output of 741-1 may be adjusted by means of the .1K potentiometer. As shown on Figure 42 B, the maximum ramp height is equal to a count of 1,023 which can be made to correspond to 1.023 volts. Then 1 volt would be equal to a count of exactly 1,000, Figure 42 B. This system would therefore be capable of determining the value of an input voltage to an accuracy of one millivolt. The design incorporates automatic polarity sensing which is achieved with the voltage comparators 741-2 and 3. The negative and positive indicators are connected directly to a nixie tube via card B 8 (see Fig. 41 A).

Since a millisecond or less is required to obtain a sample with this voltmeter, it would be possible to sample many more analog data sources with this unit. At present there are only two as noted previously, but if there were more, the addition of a more complex multiplexer would make it possible to sample more analog data sources, thus greatly increasing the versatility of this data gathering system.

Figure 38 which has been referred to previously contains the inter-card wiring information for the system as it exists at present.

The Mixer and Low Pass Filters, No. 1 and No. 2

The rubidium vapour magnetometer output signal is in the order of 80 to 350 KHz, the signal frequency being directly proportional to the magnetic field in which the magnetometer is operating. The relationship between the magnetic field and the rubidium oscillator frequency being approximately 4.66 cycles per second per gamma. In the Ottawa area, where the earth's magnetic field intensity is about 58,000 gammas, the output signal should then be about 270,280 cycles per second. If this signal is counted by a frequency counter directly, the best determination of the earth's field would be ± 0.214 gamma.

This is not good enough for high resolution magnetometer survey work. To improve the accuracy, frequency multipliers may be used. Multiplying the frequency directly results in rather high frequencies, therefore the rubidium signal is mixed with a fixed standard thus producing a difference frequency signal that will be easier to handle. The frequency synthesizer used in this system is capable of producing a signal of any desired frequency from a few cycles per second to 2 MHz. These signals are extremely stable and are based upon the crystal oscillator, the stability of which has already been noted, under the heading of "The Digital Clock". The mixer and low pass filter shown in Figure 43 accept the rubidium vapour magnetometer and the frequency synthesizer signals. The Schmitt-trigger circuits 914-1 and 914-2 convert the sine wave signals to square waves. The exclusive OR gate composed of modules 914-3 and 914-4 together with the UTC FLL 50 K filter produce a signal that can vary from 0-60 KHz. The signal level is boosted by the transistor amplifier network composed of T_1, T_2 and T_3. The output of this last stage can be fed to a frequency multiplier system which can improve the resolution to almost any desired degree. Two of these mixer, filter circuits have been included in the system so that two magnetometers may be operated simultaneously at a later date in a gradiometer configuration. Near Ottawa therefore, the frequency synthesizer may be set at any frequency between 210,28 Hz and 330,280 Hz to generate an acceptable 0-60 KHz difference frequency. This range however should be restricted to a range from 20-60 KHz depending upon the multiplier capabilities which is discussed next.

The Phase Lock Tracking Filters, No. 1 and No. 2

As suggested in the previous section, a circuit is required that is capable of multiplying the output signal of the mixer and low pass filter, thus improving the sensitivity of the magnetometer system. The "phase lock tracking filter" described here, Figures 32, 44A, 44B, 45A and 45B is capable of multiplying the input signal, f_{IN}, and following almost all of the input signal's variations in frequency. The frequency range over which the input signal may vary is from 10 to 40 KHz when the input signal frequency is being multiplied by 512, and from 20 to 80 KHz when the input signal frequency is multiplied by 256.

When using the multiplication factor of 512 the resolution is $1/(4.66 \times 512) = \pm 0.00042\gamma$. To obtain this sensitivity, the sampling interval has to be one second. For survey purposes this results in too slow a system, hence the actual sampling interval may be 0.1 or 0.2 second. This reduces the accuracy by a factor of 10 and 5, to ± 0.0042 and ± 0.0021 gammas

respectively. Using the multiplication factor of 256 doubles the range of the acceptable input signal frequency but reduces the sensitivity by one half. The practical sensitivity would then be reduced to $\pm$ 0.0084 and $\pm$ 0.0042 gammas for sampling intervals of 0.1 and 0.2 second.

The phase lock tracking filter consists of the following basic components or circuits, a voltage controlled multivibrator (VCM) a divider chain, a phase comparator and a DC voltage amplifier. The VCM has been designed to operate in the frequency range of 5 to 30 MHz, the frequency being controlled by the voltage applied to the bases of the two transistors, T_1 and T_2. These transistors were chosen for their high gain and capability to operate at high frequencies. The output of the VCM goes to the divider chain via the 900-1 module which acts as a buffer. The divider chain is composed of three types of $\div$ 2 modules (Fig. 44A). The 950 modules being capable of operating to about 50 MHz, the 926 modules to about 15 MHz and the 923 modules to about 7 MHz. Since there are nine divider modules, the output frequency will be the VCM frequency divided by 512. A later version of this circuit, Figure 44B, uses two 938 modules and one 923 module to obtain the same division, each 839 divides its input frequency by 16.

When first turned on, the output of the divider chain, f_2, will be in the frequency range of the signal arriving from the amplifier section of the mixer and low pass filter circuit, f_{IN}. The Schmitt-trigger (ST) circuit, module 91401, squares up this last mentioned input signal and produces f_1. The two signals f_1 and f_2 are then compared in one half of module 914-3, the output of which will consist of a series of pulses, f_3. The width of these pulses will depend upon the phase relationship between the two input signals. The output of the phase comparator is amplified and inverted 180 degrees by T_3. As the frequency f_1 increases, the voltage applied to the bases of T_1 and T_2 must be increased so that f_2 will also increase. For the system to operate, f_2 must increase with f_1. As f_1 increases in frequency, the pulse width of f_3 decreases. The inversion taking place in T_3 causes ever wider positive pulses to be applied to the noninverting input of the summing amplifier 741-1. The correct voltage will therefore appear at the bases of the VCM to move the operating frequency in the desired direction.

It is very important that the phase lock tracking filter acquire or lock onto the signal f_{IN} immediately after it is applied to the input of 914-1. In order that the output of the divider chain, f_2, will be close to the signal f_1 another signal path has been provided consisting of the one shot multivibrator 914-2, T_4 and the negative input of the operational amplifier 741-1. The one shot produces a series of pulses whose width has been adjusted by the choice of the resistor and capacitor attached to that circuit. That portion of the DC voltage produced at the bases of the VCM by this path is strictly frequency dependent, the voltage increasing nearly linearly with increasing frequency. The control voltage supplied by this path is set by the 50 K potentiometer in such a way that f_2 will approach f_1, but will never be quite equal to it.

The action of the phase comparator then takes over and produces the final correcting voltage that will bring f_2 into exact alignment with f_1. As long as f_1 is anywhere within the operating range noted above, the signal will be acquired within a few milliseconds. This ensures that normal operation will be resumed as soon as f_{IN} re-appears if it should have disappeared for any reason such as the momentary blockage of the rubidium vapour magnetometer by radio transmissions.

The output of the phase lock tracking filter is fed to a high speed counter incorporated in the digital system via the buffer amplifier 900-2. Figures 45A and 45B show the component layout of the card and the inter card wiring is shown on Figure 32. Two phase lock tracking filters are included in the system, one to handle the signal from the inboard magnetometer, the second to handle the signal from the magnetometer that may be installed in a bird at a later date.

High Speed Counters Nos. 1, 2 and 3

Three identical, high speed counters have been incorporated in the system. The signals from the two phase lock tracking filters are fed to counters No. 2 and 3. Counter No. 1 has been left free to sample and monitor any other signal source as required during the survey.

These counters have been designed with features common to many counters that are available commercially but they also have features that were considered desirable, but not available, on all. Some counters have a waiting period after the count command has been received that permits the signal transients to decay before the measurement is actually made. This feature has been retained, but the delay has been shortened from 0.2 second to 0.1 second. The counter makes use of memory elements that make the latest count available in digital form and as a visual display until the new count is complete. This feature permits data to be recorded while the new count is being made. It also permits data recording at a much faster rate than is possible when using counters such as the Hewlett Packard models which do not have this feature.

The counting intervals are 0.001, 0.01, 0.1, 0.2, 1.0 and 10.0 seconds which are selectable by means of SWC-11,,SWC-13 and SWC-15 for counters 1, 2 and 3 respectively (Fig. 46). Another feature that most commercial counters do not have, but which has been incorporated is a choice of pulses for resetting or initiating the count, achieved with SWC-19, SWC-21 and SWC-23 for counters 1, 2 and 3 (Figure 46). The counters may be reset by pulses coming from the digital clock at either one half or one second intervals or they may be reset once per scan as described in the discussion of the master recorder control. When surveying, this would be the mode that has to be used for those counters whose data is being recorded, because the data sampling rate would then be synchronized with the recording system. For checking purposes the count may be initiated manually by means of SWC-4, SWC-6 and SWC-8 for counters 1, 2 and 3 respectively. In addition the count may be initiated by setting the reset interval selector switch to position three. The reset pulses then come from a free running multivibrator 914-8 whose frequency may be adjusted by means of SWC-20, SWC-22 and SWC-24 for counters 1, 2 and 3.

It is possible to connect several data sources to the input of each one of the counters simultaneously, and then select the required input by means of an input selector switch, SWC-12, SWC-14 and SWC-16 for counters 1, 2 and 3 (Fig. 47). Switches SWC-27, SWC-28 and SWC-29 permit the counters to receive a calibration signal or an external signal of a relatively low frequency, from a few cycles per second to about 3 MHz.

Each counter consists of four cards, C 1-4 for No. 1, C 5-8 for No. 2 and C 9-12 for No. 3. Figure 46 shows the control card. This produces the pulses required to control and time the counting interval. The frequency standard is the same one that is used for the digital clock and digital volt meter, namely the crystal oscillator in the frequency synthesizer whose frequency stability has already been noted (see "The Digital Clock"). Referring to Figure 46, an initiate pulse entering the OS, 914-6 produces a sharp pulse that sets FF, 914-7 and applies a reset pulse to the 923 modules. This sets the output, pin 7, of the 923 modules to zero (Fig. 48). Pin 7 of 914-7 also goes to zero, which opens gate 914-1 (output pin 6); this permits the 1 MHz pulses to enter the timing counter section 958-1 to 958-7. The pulse that resets the 923 modules is also applied to all of the counter modules shown on Figure 47.

After 0.1 second, pin 1 of the OS, 914-5 goes positive, which triggers this unit, and a sharp pulse is produced. This resets the timing counters to zero and sets FF, 914-12 which causes the counter inhibit line to go negative, thus opening the counter input gate 914-17 (Fig. 47). The output pulse from 914-5 also toggles the 923-2 module, which reverses the polarity of pins 5 and 7 of that module. After this, the OS, 914-5 cannot be triggered except via the gate 914-3 (output pin 7) which is in series with the count time switch (Fig. 46). At the end of the preselected count interval, say 1.0 seconds as shown in Figure 46, the OS, 914-5 again produces a pulse. This resets the timing counters to zero, resets FF, 914-12 which inhibits the main counter input section and also causes the OS, 914-15 to produce a pulse that enters or transfers the information of the main counter stages to the 959 memory units. The latest count will then be displayed visually by the nixie tubes on the front panel of the C chassis and is also available in digital form for recording purposes.

For survey purposes a count time of 0.2 second has been found to be rather useful. To obtain this, module 923-1 has been incorporated in the design. This unit is toggled at 0.1 second intervals when the timing counter is in operation and determining the time that the main counter will be open. It cannot be toggled by the initial 0.1 second interval because of the gate 914-2 (output pin 6) which is blocked during this interval. Since the 923-1 module produces one pulse out for two pulses in, it can therefore be used to provide the 0.2 second count time interval when inserted in the circuit as shown in Figure 46. The switches SWC-5, SWC-7 and SWC-9 permit the selection of a count interval of 1.0 seconds or 0.2 second when switches SWC-11, SWC-13 and SWC-15 are in the position shown in the diagram (Fig. 46).

Figure 49 shows the card layout for the counters. The bottom right hand corner shows a schematic that indicates how the 180 V supply is turned on to supply power to the nixie display tubes. This same type of wiring is also used on the A and B chassis which also incorporates nixie display circuits.

Figure 50 shows the wiring of the various switches, required to operate the counters. Figures 51, 52 and 53 show the intercard wiring of counters 1, 2 and 3 respectively.

Shaft Position Encoders (Model 13-501A-11)

Shaft position encoders can be extremely useful tools in electro-mechanical systems. By means of them minute shaft rotations may be precisely defined in digital form. The Datex shaft position encoders used here are capable of defining one thousandth part of a revolution. They provide the information for a five numeral display, twenty bits, in a unique code adopted by the Datex engineers.

Figure 54 shows that, functionally, the Datex encoder can be compared to a group of switches that open and close to generate this code. Each switch contact is a brush that makes and breaks a connection on a track described or shown on Figure 55 which depicts the contact arrangement required to generate the datex code.

The shaft position encoders can be connected to navigation aides such as a compass, decca navigator, Loran, etc., that provide the position information to locate the aircraft or other vehicle in a horizontal plane. If properly done, the information describing the aircraft's position will be available in digital form and can be recorded along with the survey data. This can make track recovery possible without using a survey camera. By providing the computer with the correct program, it can then reproduce the flight lines to any desired scale. This has proved to be very useful for flight path recovery over water, but could also be extended to use over land. It would eliminate the tedious step of transferring the flight path from photos to a map. During the summer of 1965 an experimental area was surveyed over Hudson Bay using this method of flight path recovery. The equipment was installed in a North Star aircraft operated by the National Aeronautical Establishment (Lyster and Bower, 1968).

Figure 55 shows that the contact arrangement provides for the Datex code to be generated in such a way that there is always at least one contact in the closed position and also that a second brush will make or break contact before the first one does so. Thus any digital code, from zero to nine will always be defined by at least one brush making contact. Another peculiarity will be noted, namely that the numbers increase from 0-9 but 10 is defined as 19, 11 as 18, 12 as 17 etc. (see the left hand two columns of Fig. 55). In order that this code may be used with more conventional recording and monitoring systems, it has to be converted into a code such as the 8-4-2-1 which has been mentioned previously.

To do this refer to the left hand portion of Figure 56. At the top left, there is a column labelled "No." and beneath it, the numbers 0-15, the sixteen possible states that four contacts can define. Immediately to the right, under the heading "ABCD", these numbers are defined in a logical sequence in digital form. Under the heading, "Datex" will be found a column of numbers and Xs. At first glance this column does not appear to have any logical sequence. It is obtained by comparing the Datex code under the heading "t_4, t_3, t_2, t_1" (Fig. 55) to the code under the "ABCD" heading (Fig. 56). Thus the natural binary code defines "0" as 0000, but the datex code does not, in fact it does not use it at all. Therefore an X is placed opposite the 0000 under the "Datex" heading. The datex equivalent of zero will be found to correspond to the ABCD code for one (0001). The datex one corresponds to the natural binary three (0011), and the datex two corresponds to the natural binary two (0010) etc. After having completed the column under the "Datex" heading make up another set of four columns under the heading of the code

that we wish to employ, in this case 8-4-2-1 (Fig. 56), and write the natural binary equivalent of the numbers opposite the Datex numbers. Thus for the first row across it will be XXXX, the second 0000, the third 0010 etc.

Next we have to find what Boolean equation, in its simplest form, will have to be implemented that will change the datex code to the 8-4-2-1 code. This may be done conveniently by means of the Karnaugh map, which in this case consists of a block of sixteen squares (Hoernes and Heilweil, n.d.). To obtain the Boolean equation that defines the "1" the "2" the "4" and the "8" see Figure 56. Figure 57 lists the Boolean equations that have to be implimented to obtain a five numeral display.

There is one more problem, which was touched on briefly, namely the fact that the Datex code consists of normal and reflected portions. By looking again at Figure 55, it may be seen that the left hand column of numbers increases in the normal fashion. Immediately to the right is another column of numbers that increase normally from 0 to 9, then the number suddenly jumps from 9 to 19. As already noted we are faced with a reflected code. To make use of this shaft position encoder, this must be corrected. The clue to this puzzle is to note that the 10^0 column is only reflected when the 10^1 column is odd, and normal when the 10^1 column is even. The same relationship holds every two adjacent columns. The top right hand portion of Figure 56 shows how this is corrected.

The left hand column is obtained from the information contained on Figure 55. Thus, when the 10^1 column is 0 or even, the 10^0 column is Normal, hence put down an N. When the 10^1 column is a 1, or odd, the 10^1 column is Reflected, write an R. In this manner under the heading of "Datex Code" we obtain two columns, one where N or R alternate opposite the column of numbers 0 to 9. Next under the heading of "ABCD" write down the code for the numbers 0 to 9 that datex uses to define these numbers. This leaves six contact possibilities where there are four contacts. Add these to the right of the two columns where there are only Xs. Under the heading of "map", write the numbers that would be defined by the normal 8-4-2-1 code. This gives the position of the N and R values on the Karnaugh map. Since nothing is wrong with the numbers designated by N, they may be replaced by an X on the Karnaugh map to simplify the Boolean equation. The equation that will correct the reflected portion that then results is given on Figure 56. The lower portion of this figure shows, by means of a logic diagram, using AND, OR logic, how the reflected portion of the datex code may be corrected. Immediately below it the same result is obtained, using NAND, NOR logic.

To differentiate between the twenty wiper or brush contacts, that generate the code, a numbering system has been introduced in which the contacts are named t_1, t_2 .... t_{20} (Fig. 55). Thus under column ABCD (Fig. 56) these letters will be found in groups of four. For 10^0 we have $t_1 - t_4$, for 10^1, $t_5 - t_8$ etc. Then to define a number 0 to 9, $t_1 - t_4$ will be used to implement it, a number 10 to 99 requires $t_5 - t_8$ etc. However because of the reflected portion of the code, instead of using t_4 directly, we must use t_4R, instead of t_8 use t_8R and for t_{16} use $t_{16}R$.

Because there are two discs in the encoder the inside tracks can be made quite simply since they will not be crowded. The contacts made by t_{12} and t_{20} therefore are unaffected and they may be used directly as the equations on Figure 57 indicate. One disc handles the numbers 0-999 and the other numbers 1,000-99,000.

Figures 58, 59 and 60 show the logic functions required to produce the number displays, 10^0 to 10^4 inclusive and the layout of these components. Card B2 was layed out somewhat differently and is shown separately on Figure 61. Figure 58 contains or shows a free running multivibrator, mounted on cards B2 and B5 only. When SWB-1 and SWB-3 (Fig. 62) are turned to the automatic mode, the data from the shaft position encoders will be entered into the display section at a rate of about 100,000 times per second. In the manual mode, the navigator has to press the momentary contact button to enter the latest information into the memory stages and into the display section. This is preferable when Loran A is used. The navigator must first set the Loran receiver controls manually to indicate the correct position. The new position is entered only when he presses the button. The recording and display sections will therefore not get the incorrect or meaningless numbers while the tuning is in process. For Loran C or the Decca Navigator or a Compass repeater where tracking is automatic the automatic sampling mode would be more desireable. Figure 62 also shows SWB-2 and SWB-4. Referring back to Figure 54 it will be seen that the shaft position encoder can be made to read up (numbers increasing) for clockwise or counter clockwise rotation of the shaft. By means of these switches the proper selection may be made. Figure 63 indicates the correct intercard wiring for the shaft position encoders.

CONCLUSIONS

What has been learned and achieved by going through this elaborate procedure of designing a compact digital system? To answer this, one has to look back to the state of the art as it pertained to digital systems in the fall of 1966 when this phase of the project began. Almost all of the equipment available at that time was designed to use transistors and other individual components to build up a system. The resultant equipment was rugged and quite light when compared to similar equipment using vacuum tubes. However it was not light and compact when compared to what could be achieved using integrated circuits that had come onto the market shortly before that time. It is the author's view that the size and weight of the equipment required to digitize and record all the pertinent parameters of a magnetometer survey could not have been fitted into an aircraft the size of the Queen Air if the system had not been redesigned with the express purpose of reducing the equipment weight and size drastically. Integrated circuitry has made this possible.

Because this project was begun when integrated circuits first came onto the market, it required that the people involved in the project had to learn how to use these new components. If nothing else had been achieved, at least this project has produced a team that is quite competent in the art of using this powerful new tool.

The most important result of this project however would be that it now is possible to use relatively small aircraft to conduct reconnaissance aeromagnetic surveys using digital recording techniques. Looked at from a cost point of view, the resultant savings which may be attributed to this use of small aircraft, instead of the large ones required previously, have made the project well worthwhile.

ACKNOWLEDGMENTS

It would have been difficult, if not impossible, to carry out this project without previous experience in the design, construction, and operation of digital data acquisition systems. This was gained by working in close cooperation with the Magnetic Anomaly Detection (MAD) Group at the National Aeronautical Establishment (NAE), a division of the National Research Council of Canada (NRC).

This group is in charge of the instrumentation of the high resolution magnetometer aircraft, the North Star, which probably has one of the most advanced and sophisticated systems in the world today. It has been an inspiration, a pleasure and a privilege of working with this dedicated group. The author would like to take this opportunity of thanking all those involved, for their assistance and encouragement.

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ABBREVIATIONS USED IN THIS REPORT

D/A	-	Digital to Analog
EOG	-	End of gate
FF	-	Flip flop
FR	-	Free running
IRG	-	Inter record gap
OS	-	One shot
PPS	-	Pulses per second
PTU	-	Pulse to unit
RR	-	Recording rate
ST	-	Schmitt trigger

No.	8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

TABLE I

8421 code

No.	PULSE	A_4	A_3	A_2	A_1
0		0	0	0	0
1	TRANS.	0	0	0	1
2	SHIFT	0	0	1	0
3	SHIFT	0	0	1	1
4	SHIFT	0	1	0	0
5	SHIFT	0	1	0	1
6	SHIFT	0	1	1	0

TABLE II

The status of the "A" counter required to produce the Transfer and Shift pulses.

GATE NO.	B_4	B_3	B_2	B_1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

TABLE III

The status of the "B" counter required to provide the gate identification.

C	B	A	8	4	2	1
-			-			-
-			-			-
-			-			-
-			-			-
-			-			-
	-		-			-

TABLE IV
(ODD PARITY)

A Bit in the "B" column indicating a gate identifier.

0000 to 0777 (Octal)	0000 to 0511 (Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
0000	0000	0001	0002	0003	0004	0005	0006	0007
0010	0008	0009	0010	0011	0012	0013	0014	0015
0020	0016	0017	0018	0019	0020	0021	0022	0023
0030	0024	0025	0026	0027	0028	0029	0030	0031
0040	0032	0033	0034	0035	0036	0037	0038	0039
0050	0040	0041	0042	0043	0044	0045	0046	0047
0060	0048	0049	0050	0051	0052	0053	0054	0055
0070	0056	0057	0058	0059	0060	0061	0062	0063
0100	0064	0065	0066	0067	0068	0069	0070	0071
0110	0072	0073	0074	0075	0076	0077	0078	0079
0120	0080	0081	0082	0083	0084	0085	0086	0087
0130	0088	0089	0090	0091	0092	0093	0094	0095
0140	0096	0097	0098	0099	0100	0101	0102	0103
0150	0104	0105	0106	0107	0108	0109	0110	0111
0160	0112	0113	0114	0115	0116	0117	0118	0119
0170	0120	0121	0122	0123	0124	0125	0126	0127
0200	0128	0129	0130	0131	0132	0133	0134	0135
0210	0136	0137	0138	0139	0140	0141	0142	0143
0220	0144	0145	0146	0147	0148	0149	0150	0151
0230	0152	0153	0154	0155	0156	0157	0158	0159
0240	0160	0161	0162	0163	0164	0165	0166	0167
0250	0168	0169	0170	0171	0172	0173	0174	0175
0260	0176	0177	0178	0179	0180	0181	0182	0183
0270	0184	0185	0186	0187	0188	0189	0190	0191
0300	0192	0193	0194	0195	0196	0197	0198	0199
0310	0200	0201	0202	0203	0204	0205	0206	0207
0320	0208	0209	0210	0211	0212	0213	0214	0215
0330	0216	0217	0218	0219	0220	0221	0222	0223
0340	0224	0225	0226	0227	0228	0229	0230	0231
0350	0232	0233	0234	0235	0236	0237	0238	0239
0360	0240	0241	0242	0243	0244	0245	0246	0247
0370	0248	0249	0250	0251	0252	0253	0254	0255

	0	1	2	3	4	5	6	7
0400	0256	0257	0258	0259	0260	0261	0262	0263
0410	0264	0265	0266	0267	0268	0269	0270	0271
0420	0272	0273	0274	0275	0276	0277	0278	0279
0430	0280	0281	0282	0283	0284	0285	0286	0287
0440	0288	0289	0290	0291	0292	0293	0294	0295
0450	0296	0297	0298	0299	0300	0301	0302	0303
0460	0304	0305	0306	0307	0308	0309	0310	0311
0470	0312	0313	0314	0315	0316	0317	0318	0319
0500	0320	0321	0322	0323	0324	0325	0326	0327
0510	0328	0329	0330	0331	0332	0333	0334	0335
0520	0336	0337	0338	0339	0340	0341	0342	0343
0530	0344	0345	0346	0347	0348	0349	0350	0351
0540	0352	0353	0354	0355	0356	0357	0358	0359
0550	0360	0361	0362	0363	0364	0365	0366	0367
0560	0368	0369	0370	0371	0372	0373	0374	0375
0570	0376	0377	0378	0379	0380	0381	0382	0383
0600	0384	0385	0386	0387	0388	0389	0390	0391
0610	0392	0393	0394	0395	0396	0397	0398	0399
0620	0400	0401	0402	0403	0404	0405	0406	0407
0630	0408	0409	0410	0411	0412	0413	0414	0415
0640	0416	0417	0418	0419	0420	0421	0422	0423
0650	0424	0425	0426	0427	0428	0429	0430	0431
0660	0432	0433	0434	0435	0436	0437	0438	0439
0670	0440	0441	0442	0443	0444	0445	0446	0447
0700	0448	0449	0450	0451	0452	0453	0454	0455
0710	0456	0457	0458	0459	0460	0461	0462	0463
0720	0464	0465	0466	0467	0468	0469	0470	0471
0730	0472	0473	0474	0475	0476	0477	0478	0479
0740	0480	0481	0482	0483	0484	0485	0486	0487
0750	0488	0489	0490	0491	0492	0493	0494	0495
0760	0496	0497	0498	0499	0500	0501	0502	0503
0770	0504	0505	0506	0507	0508	0509	0510	0511

1000 to 1777 (Octal)	0512 to 1023 (Decimal)

	0	1	2	3	4	5	6	7
1000	0512	0513	0514	0515	0516	0517	0518	0519
1010	0520	0521	0522	0523	0524	0525	0526	0527
1020	0528	0529	0530	0531	0532	0533	0534	0535
1030	0536	0537	0538	0539	0540	0541	0542	0543
1040	0544	0545	0546	0547	0548	0549	0550	0551
1050	0552	0553	0554	0555	0556	0557	0558	0559
1060	0560	0561	0562	0563	0564	0565	0566	0567
1070	0568	0569	0570	0571	0572	0573	0574	0575
1100	0576	0577	0578	0579	0580	0581	0582	0583
1110	0584	0585	0586	0587	0588	0589	0590	0591
1120	0592	0593	0594	0595	0596	0597	0598	0599
1130	0600	0601	0602	0603	0604	0605	0606	0607
1140	0608	0609	0610	0611	0612	0613	0614	0615
1150	0616	0617	0618	0619	0620	0621	0622	0623
1160	0624	0625	0626	0627	0628	0629	0630	0631
1170	0632	0633	0634	0635	0636	0637	0638	0639
1200	0640	0641	0642	0643	0644	0645	0646	0647
1210	0648	0649	0650	0651	0652	0653	0654	0655
1220	0656	0657	0658	0659	0660	0661	0662	0663
1230	0664	0665	0666	0667	0668	0669	0670	0671
1240	0672	0673	0674	0675	0676	0677	0678	0679
1250	0680	0681	0682	0683	0684	0685	0686	0687
1260	0688	0689	0690	0691	0692	0693	0694	0695
1270	0696	0697	0698	0699	0700	0701	0702	0703
1300	0704	0705	0706	0707	0708	0709	0710	0711
1310	0712	0713	0714	0715	0716	0717	0718	0719
1320	0720	0721	0722	0723	0724	0725	0726	0727
1330	0728	0729	0730	0731	0732	0733	0734	0735
1340	0736	0737	0738	0739	0740	0741	0742	0743
1350	0744	0745	0746	0747	0748	0749	0750	0751
1360	0752	0753	0754	0755	0756	0757	0758	0759
1370	0760	0761	0762	0763	0764	0765	0766	0767

	0	1	2	3	4	5	6	7
1400	0768	0769	0770	0771	0772	0773	0774	0775
1410	0776	0777	0778	0779	0780	0781	0782	0783
1420	0784	0785	0786	0787	0788	0789	0790	0791
1430	0792	0793	0794	0795	0796	0797	0798	0799
1440	0800	0801	0802	0803	0804	0805	0806	0807
1450	0808	0809	0810	0811	0812	0813	0814	0815
1460	0816	0817	0818	0819	0820	0821	0822	0823
1470	0824	0825	0826	0827	0828	0829	0830	0831
1500	0832	0833	0834	0835	0836	0837	0838	0839
1510	0840	0841	0842	0843	0844	0845	0846	0847
1520	0848	0849	0850	0851	0852	0853	0854	0855
1530	0856	0857	0858	0859	0860	0861	0862	0863
1540	0864	0865	0866	0867	0868	0869	0870	0871
1550	0872	0873	0874	0875	0876	0877	0878	0879
1560	0880	0881	0882	0883	0884	0885	0886	0887
1570	0888	0889	0890	0891	0892	0893	0894	0895
1600	0896	0897	0898	0899	0900	0901	0902	0903
1610	0904	0905	0906	0907	0908	0909	0910	0911
1620	0912	0913	0914	0915	0916	0917	0918	0919
1630	0920	0921	0922	0923	0924	0925	0926	0927
1640	0928	0929	0930	0931	0932	0933	0934	0935
1650	0936	0937	0938	0939	0940	0941	0942	0943
1660	0944	0945	0946	0947	0948	0949	0950	0951
1670	0952	0953	0954	0955	0956	0957	0958	0959
1700	0960	0961	0962	0963	0964	0965	0966	0967
1710	0968	0969	0970	0971	0972	0973	0974	0975
1720	0976	0977	0978	0979	0980	0981	0982	0983
1730	0984	0985	0986	0987	0988	0989	0990	0991
1740	0992	0993	0994	0995	0996	0997	0998	0999
1750	1000	1001	1002	1003	1004	1005	1006	1007
1760	1008	1009	1010	1011	1012	1013	1014	1015
1770	1016	1017	1018	1019	1020	1021	1022	1023

Table V. An octal to decimal conversion table.

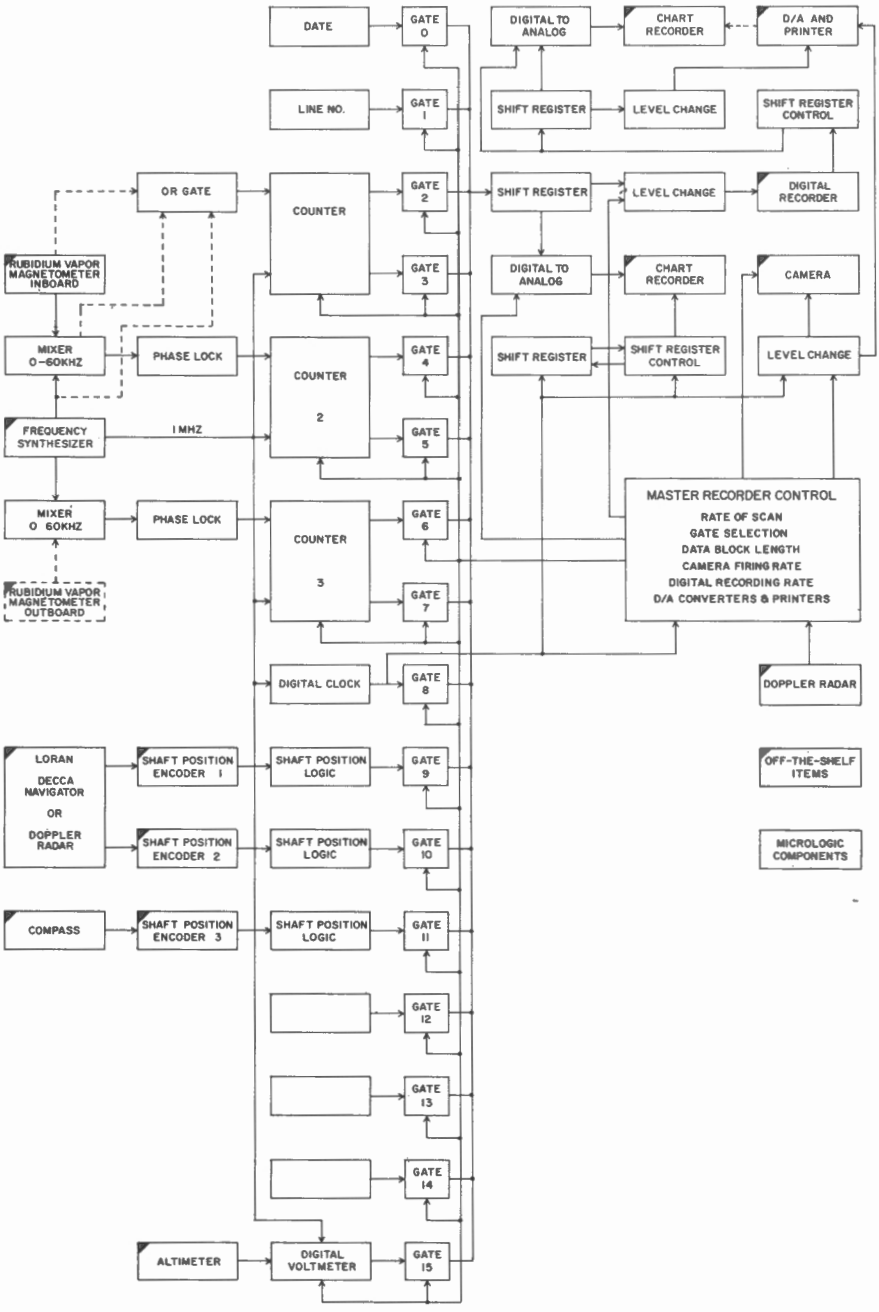
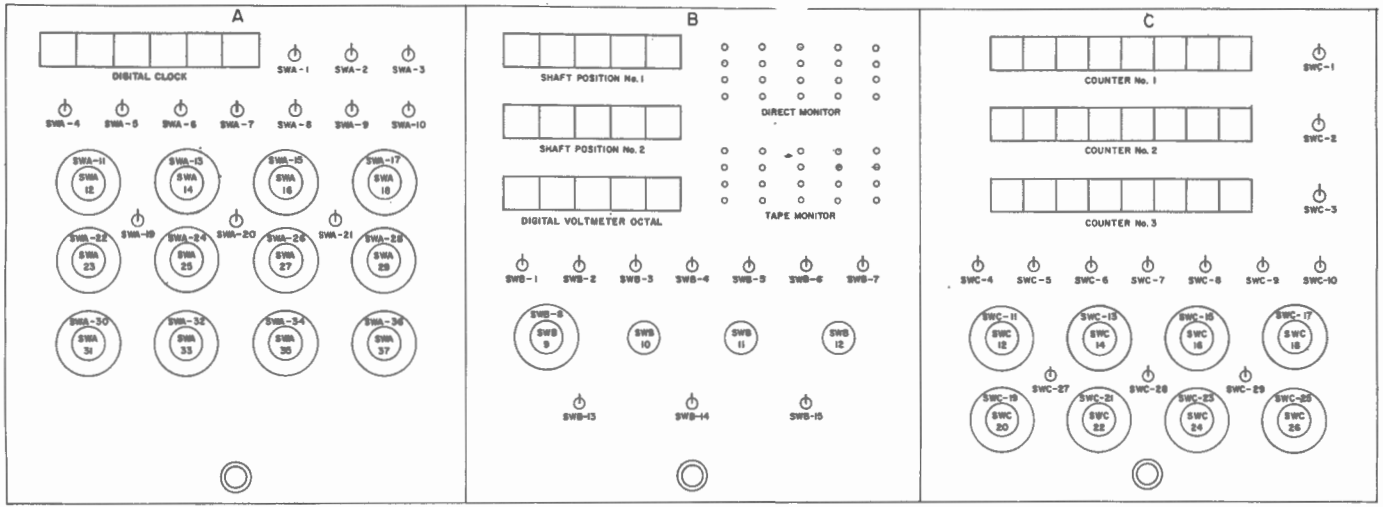


Figure 1. Block diagram of the digital recording system.

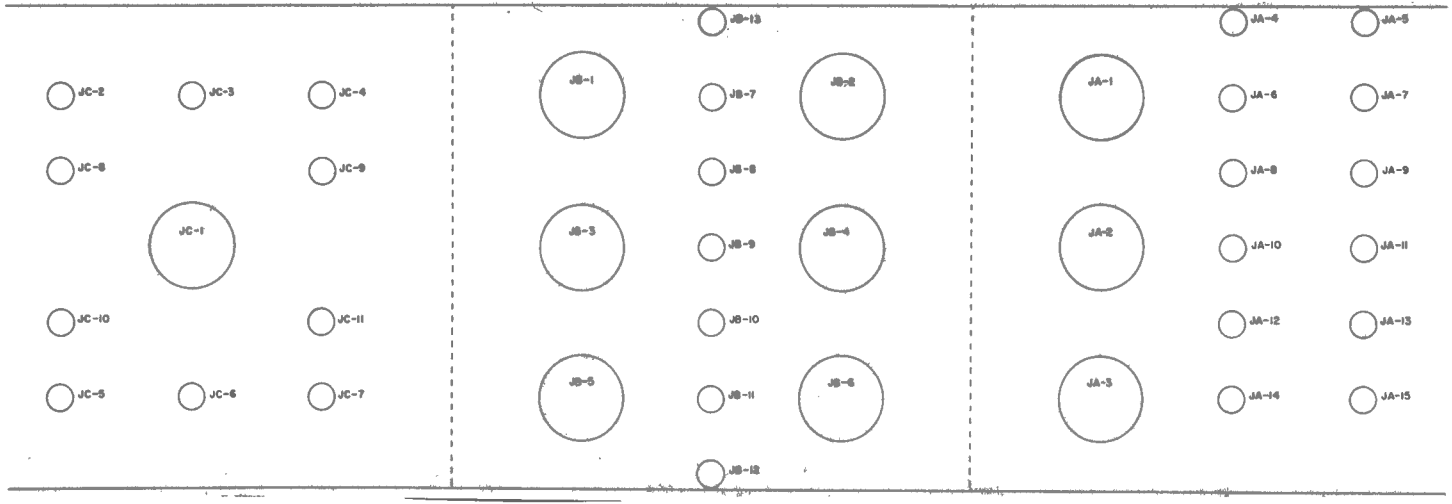


SWA-1; DN, SET TIME OF DAY. UP, OPERATE
SWA-2; DN, RETARD, UP ADVANCE
SWA-3; DN, SLOW, UP, FAST
SWA-4; 10 KPPS
SWA-5; 1 KPPS
SWA-6; .1 KPPS
SWA-7; .01 KPPS
SWA-8; .001 KPPS
SWA-9; DN, PWR OFF, UP, PWR ON
SWA-10; UP 100 PPS (CLOCK)
DOWN 2000 P.P.M. (DOPPLER)
SWA-11; GATE 0
SWA-12; GATE 1
SWA-13; GATE 2
SWA-14; GATE 3
SWA-15; GATE 4
SWA-16; GATE 5
SWA-17; GATE 6
SWA-18; GATE 7
SWA-19; MAN, RATE OF SCAN RESET (TEST)
SWA-20; MAN, RECORDING RATE (TEST)
SWA-21;
SWA-22; GATE 8
SWA-23; GATE 9
SWA-24; GATE 10
SWA-25; GATE 11
SWA-26; GATE 12
SWA-27; GATE 13
SWA-28; GATE 14
SWA-29; GATE 15
SWA-30; RATE OF SCAN
SWA-31; SELECT RECORDING RATE
SWA-32; PTU SELECTOR SWITCH
SWA-33; (DIRECT MONITOR)
SWA-34; CAMERA PULSE RATE
SWA-35; BLOCK LENGTH SELECTOR
SWA-36;
SWA-37;
SWA-38; NAV. OP. CAMERA

SWB-1; S.P. #1 OP. MODE UP AUTO
DOWN MANUAL
SWB-2; S.P. #1 POLARITY SELECT
SWB-3; S.P. #2 OP. MODE UP AUTO
DOWN MANUAL
SWB-4; S.P. #2 POLARITY SELECT
SWB-5; D.V.M. UP MANUAL RESET
SWB-6;
SWB-7;
SWB-8; P.T.U. SELECTOR SW. 0-15
SWB-9; (TAPE MONITOR)
SWB-10; D.V.M. SCALE SELECT
SWB-11; D/A DIRECT MONITOR
SWB-12; D/A TAPE MONITOR
SWB-13; S.P. #1 PWR UP ON DOWN OFF
SWB-14; S.P. #2 PWR UP ON DOWN OFF
SWB-15; DVM PWR UP ON DOWN OFF

SWC-1; CNTR #1 PWR UP ON DOWN OFF
SWC-2; CNTR #2 PWR UP ON DOWN OFF
SWC-3; CNTR #3 PWR UP ON DOWN OFF
SWC-4; CNTR #1 UP MANUAL RESET
SWC-5; CNTR #1 UP 1_S DOWN $.2_S$
SWC-6; CNTR #2 UP MANUAL RESET
SWC-7; CNTR #2 UP 1_S DOWN $.2_S$
SWC-8; CNTR #3 UP MANUAL RESET
SWC-9; CNTR #3 UP 1_S DOWN $.2_S$
SWC-10; Ø LOCK PWR UP ON DOWN OFF
SWC-11; CNTR #1 COUNT TIME SEL. SW.
SWC-12; CNTR #1 INPUT SEL. SW.
SWC-13; CNTR #2 COUNT TIME SEL. SW.
SWC-14; CNTR #2 INPUT SEL. SW.
SWC-15; CNTR #3 COUNT TIME SEL. SW.
SWC-16; CNTR #3 INPUT SEL. SW.
SWC-17;
SWC-18;
SWC-19; CNTR #1 RESET INTERVAL SEL. SW.
SWC-20; CNTR #1 INTERVAL RESET INTERVAL
SWC-21; CNTR #2 RESET INTERVAL SEL. SW.
SWC-22; CNTR #2 INTERNAL RESET INTERVAL
SWC-23; CNTR #3 RESET INTERVAL SEL. SW.
SWC-24; CNTR #3
SWC-25;
SWC-26;
SWC-27; CNTR #1 UP OPERATE
DOWN CALIBRATE
SWC-28; CNTR #2 UP OPERATE
DOWN CALIBRATE
SWC-29; CNTR #3 UP OPERATE
DOWN CALIBRATE

Figure 2. Front view of the digital chassis.



JC- 1; MS3102A-14P, POWER: 0v,o5v, PWERR: 0v,o5v, olwv,-6v

JC- 1; MS3102A-14P, POWER: 0v, +6v, +12v, -6v
JC- 2; BNC, MIXED SIG. IN →ØL C14-47
JC- 3; BNC, 1-30MC/S IN →C6-8
JC- 4; BNC, 100C/S-2MC/S→C6-2 VIA SWC-28
JC- 5; BNC, MIXED SIG. IN →ØL C16-47
JC- 6; BNC, 1-30MC/S IN →C10-8
JC- 7; BNC, 100C/S-2MC/S IN →C10-2 VIA SWC-29
JC- 8; BNC, 1MC/S XTAL →C9-48
JC- 9; BNC, 1-30MC/S IN →C2-8
JC-10; BNC, 100C/S-2MC/S →C2-2 VIA SWC-27
JC-11; BNC, 1-30MC/S→C2-4

JB- 1; PTO2CE-18-30PX, FROM SHAFT POSN. ENCODER # 1
JB- 2; PTO2CE-18-30PW, FROM SHAFT POSN. ENCODER # 2
JB- 3; PTO2CE-18-30P, TO/FROM KENNEDY RECORDER (P1)
JB- 4; PTO2CE-18-32P, TO TOP H.P. J101/DIR. MONITOR
JB- 5; PTO2CE-18-32P, TO TOP H.P. J101 TAPE MONITOR
JB- 6; PTO2CE-18-32PW, TO BOTM. H.P. J101 (TIME CODE)
JB- 7; BNC, ANALOG VOLTAGE IN (ALT)
JB- 8; BNC, D/A ANALOG OUT, DIRECT MONITOR
JB- 9; BNC, D/A ANALOG OUT, TAPE MONITOR
JB-10; BNC, MANUAL SAMPLE PULSE, S.P. ENCODERS
JB-11; BNC, 1MC → B7-5
JB-12; BNC, MANUAL SAMPLE PULSE S.P. ENCODERS
JB-13; BNC, ANALOG V. ACR. TRK

JA- 1; PTO2CE-22-55P, DATE CODE FOR GATE # 0, LINE NO. CODE FOR GATE # 1
JA- 2; PTO2CE-18-30Y, TIM CODE FOR CAMERA
JA- 3; PTO2CE-16-8Y, 117VAC, 400C/S
JA- 4; BNC, 1MC/S SIGNAL IN FROM SIGNAL GENERATOR
JA- 5; BNC, 1MC OUT
JA- 6; BNC, DOPPLER MILE PULSES IN
JA- 7; BNC, DOPPLER DRIFT PULSES IN
JA- 8; BNC, 1PPS OUT
JA- 9; BNC, 2PPS OUT
JA-10; BNC, 10PPS OUT
JA-11; BNC, 1PP10S OUT
JA-12; BNC, TIME CODE (RECORDER)
JA-13; BNC, DOPPLER MILE PULSES OUT (RECORDER)
JA-14; BNC, CAMERA FIRING PULSES
JA-15; BNC, MANUAL CAMERA OPERATION

Figure 3. Rear view of the digital chassis.

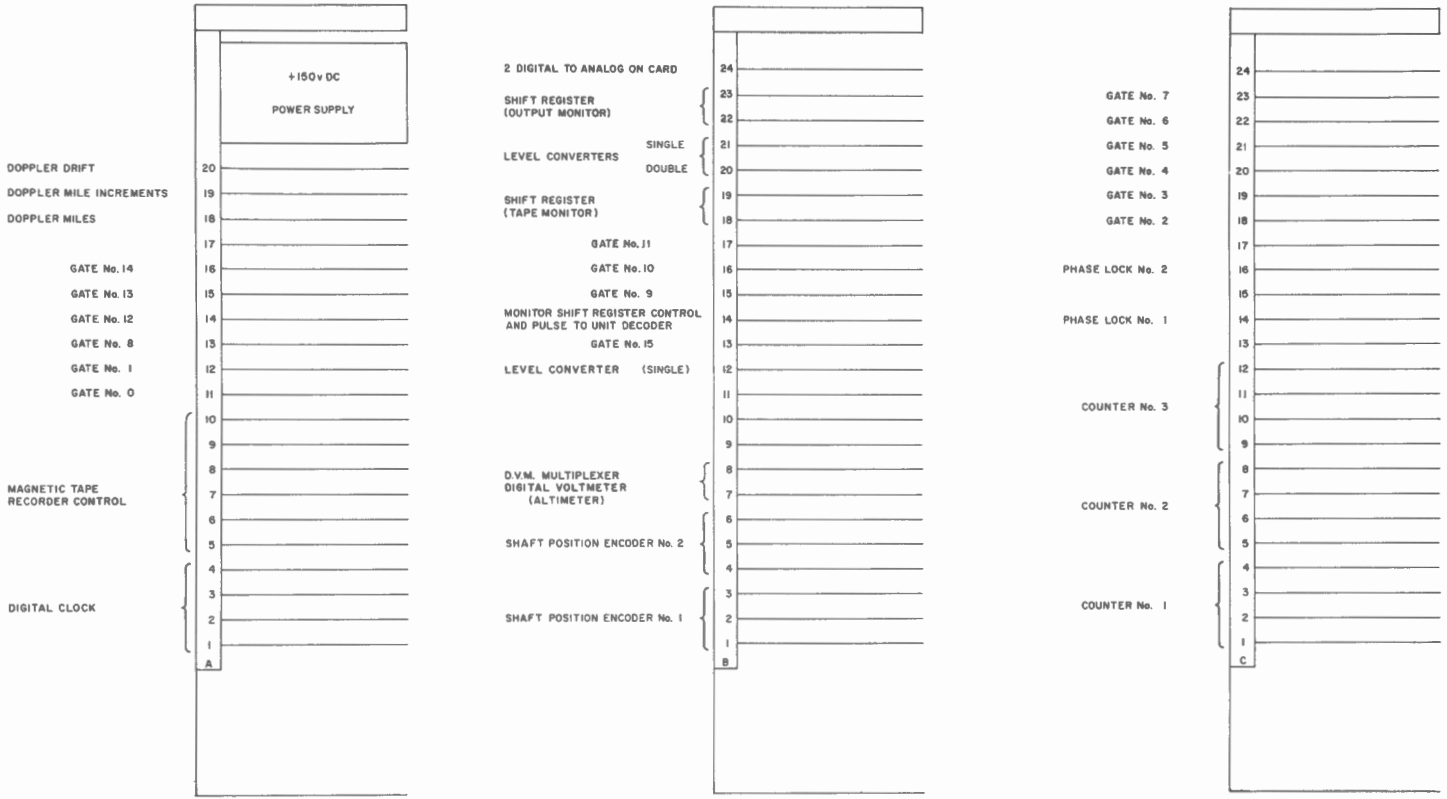


Figure 4. Top view of the digital chassis.

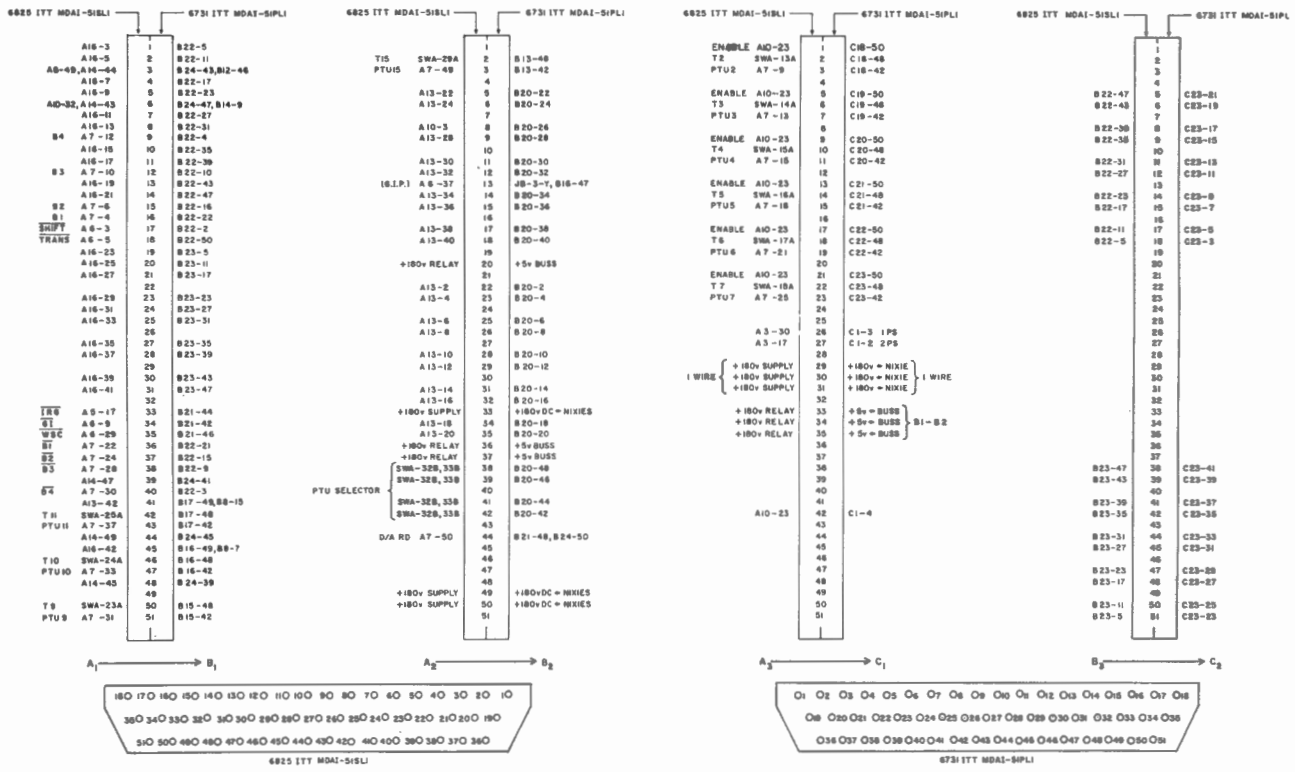


Figure 5. Diagram of the digital interchassis cabling.

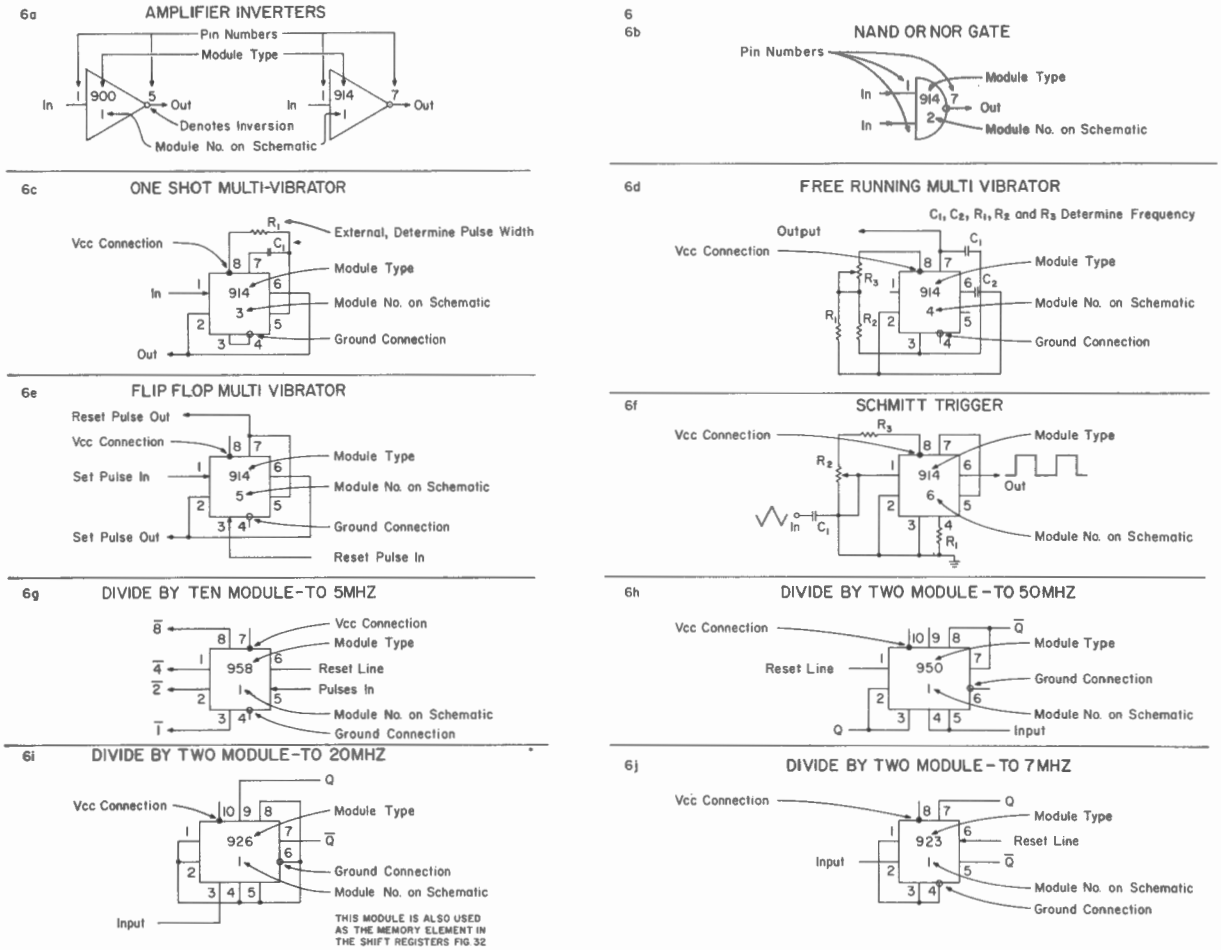


Figure 6. Connections for the more common micrologic modules.

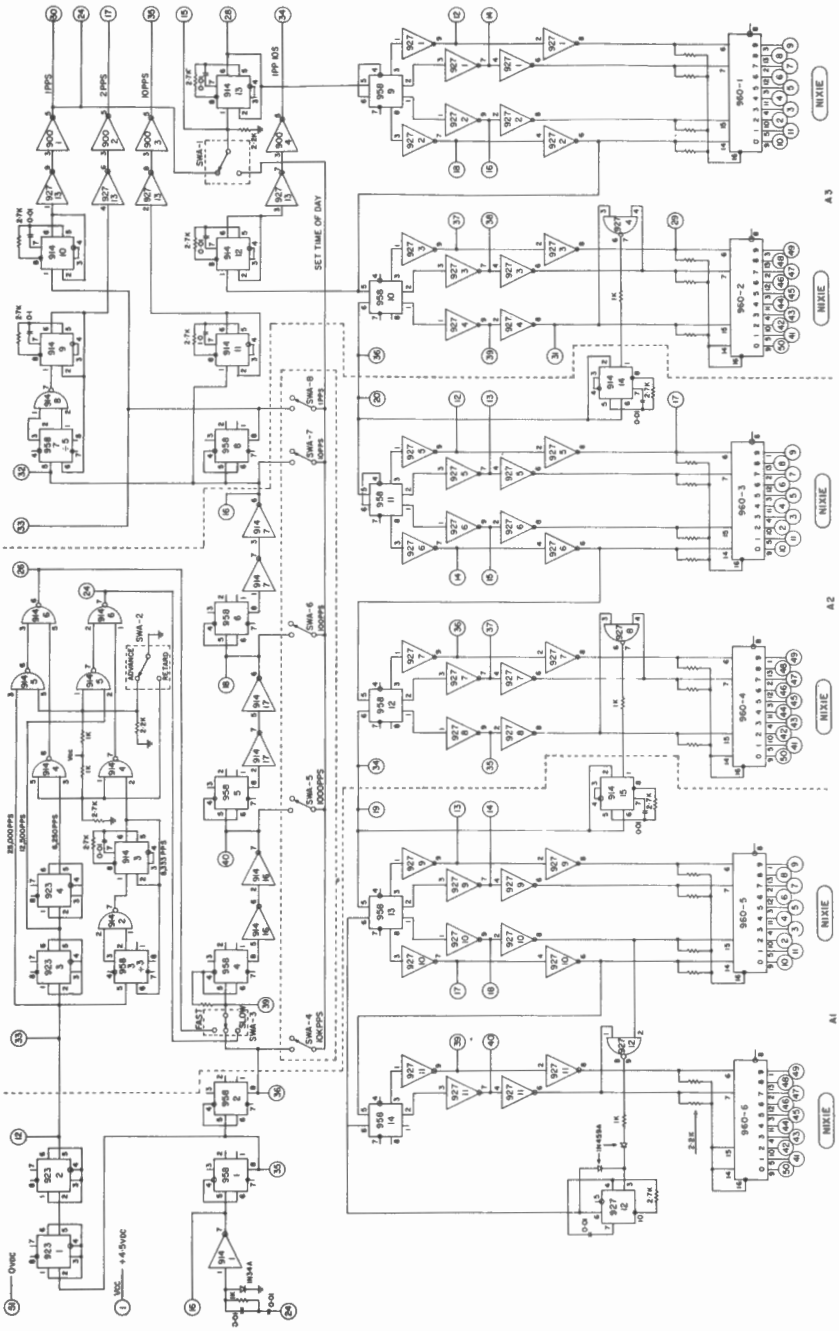


Figure 7. Digital clock display logic and countdown sequence.

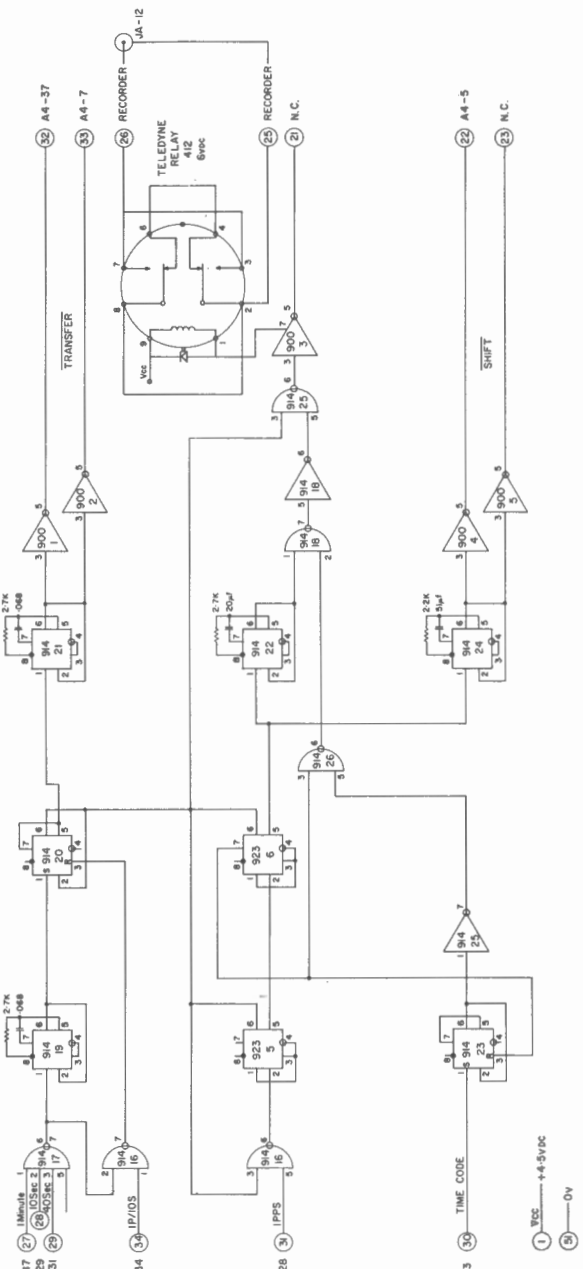


Figure 8. Digital clock time code shift register control.

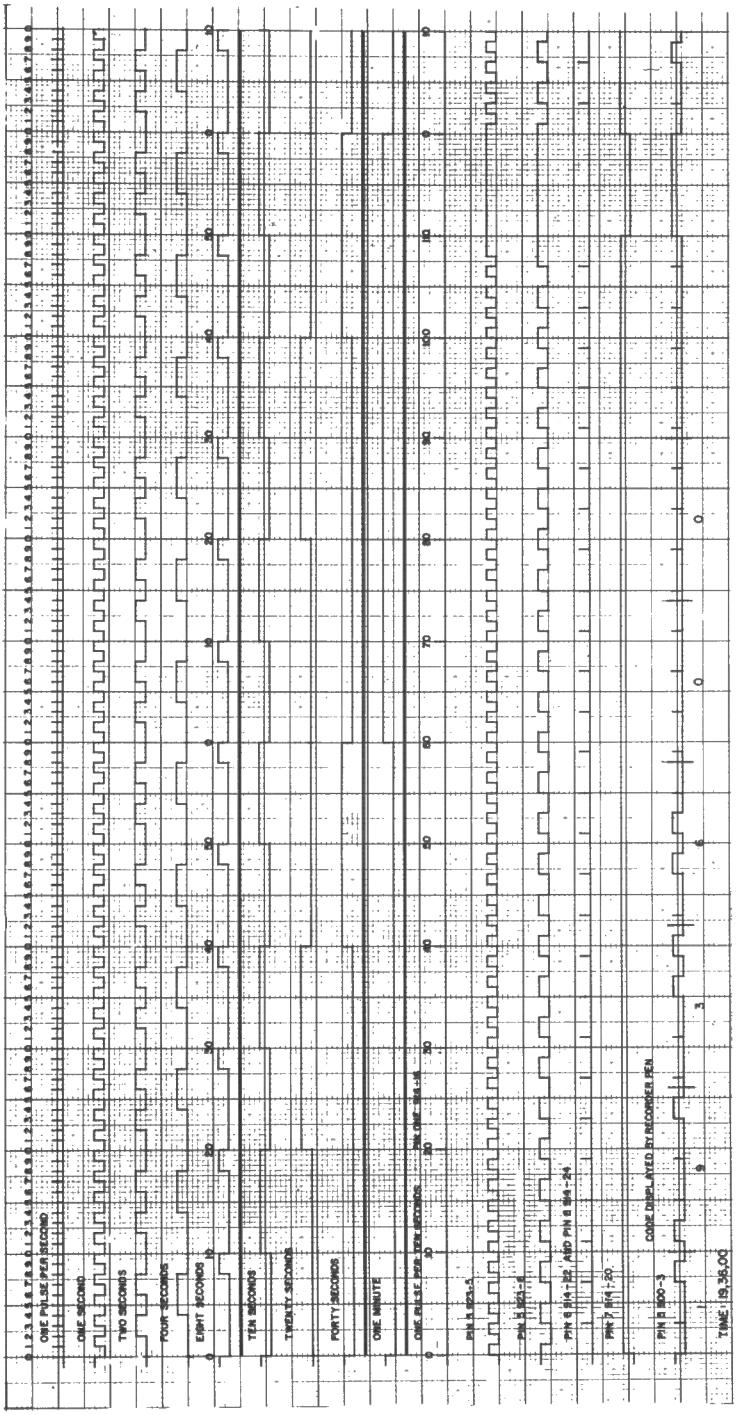


Figure 9. Digital clock timing diagram.

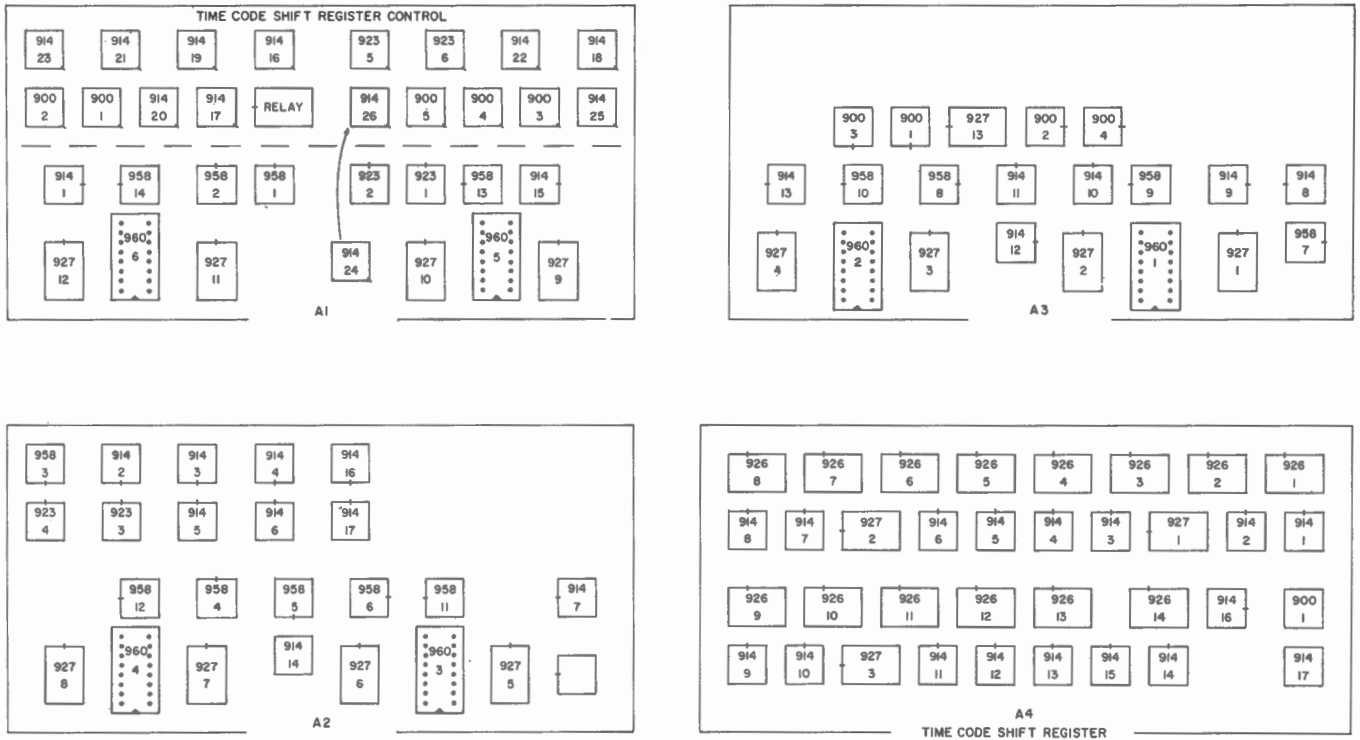


Figure 10. Digital clock card layout.

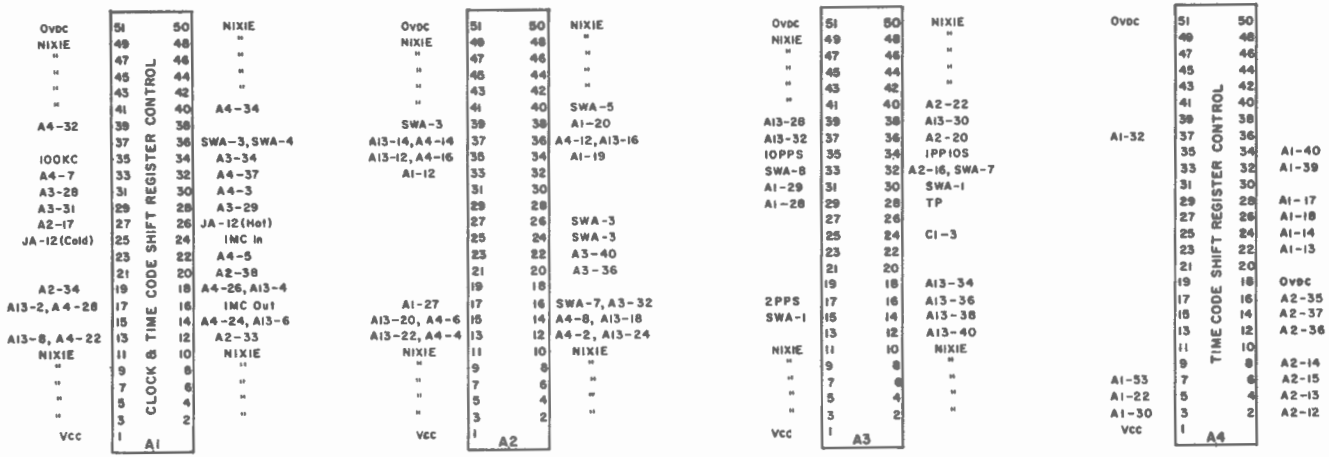


Figure 11. Digital clock intercard wiring.

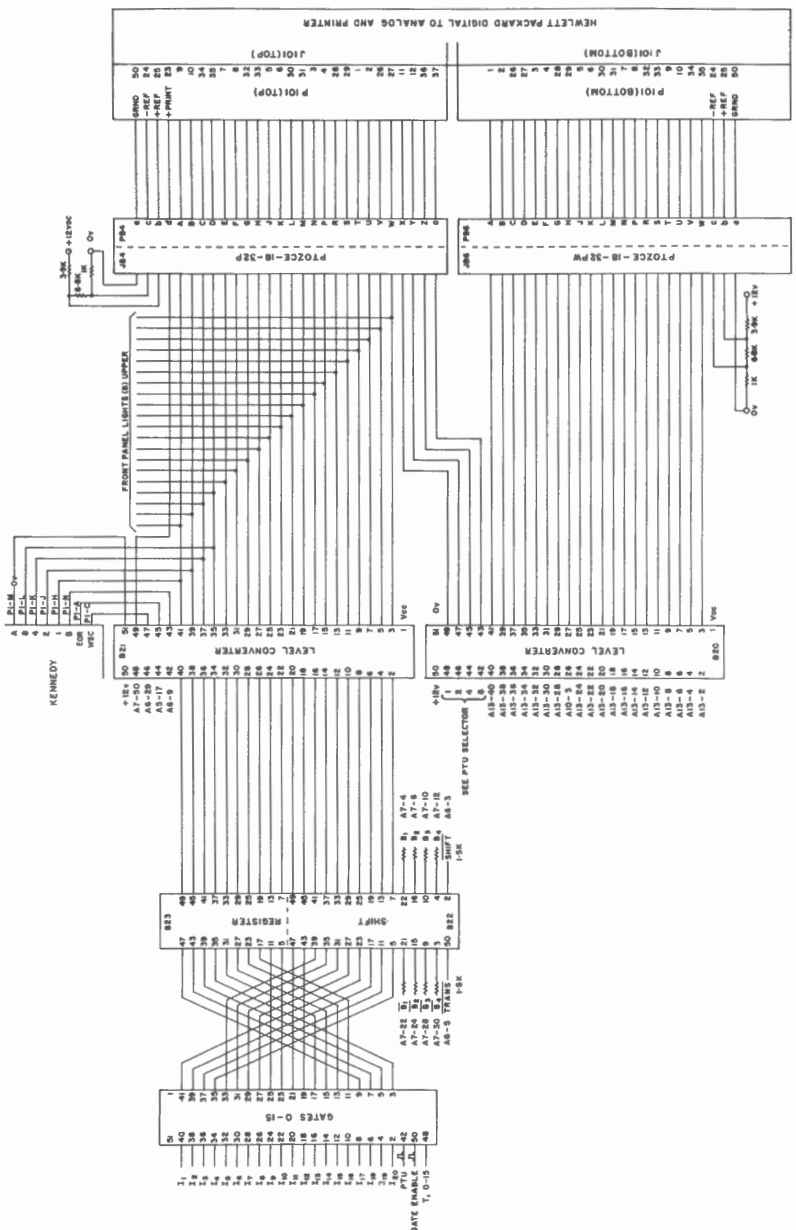


Figure 12. Time and data to the shift register and to the digital to analog converter and printer.

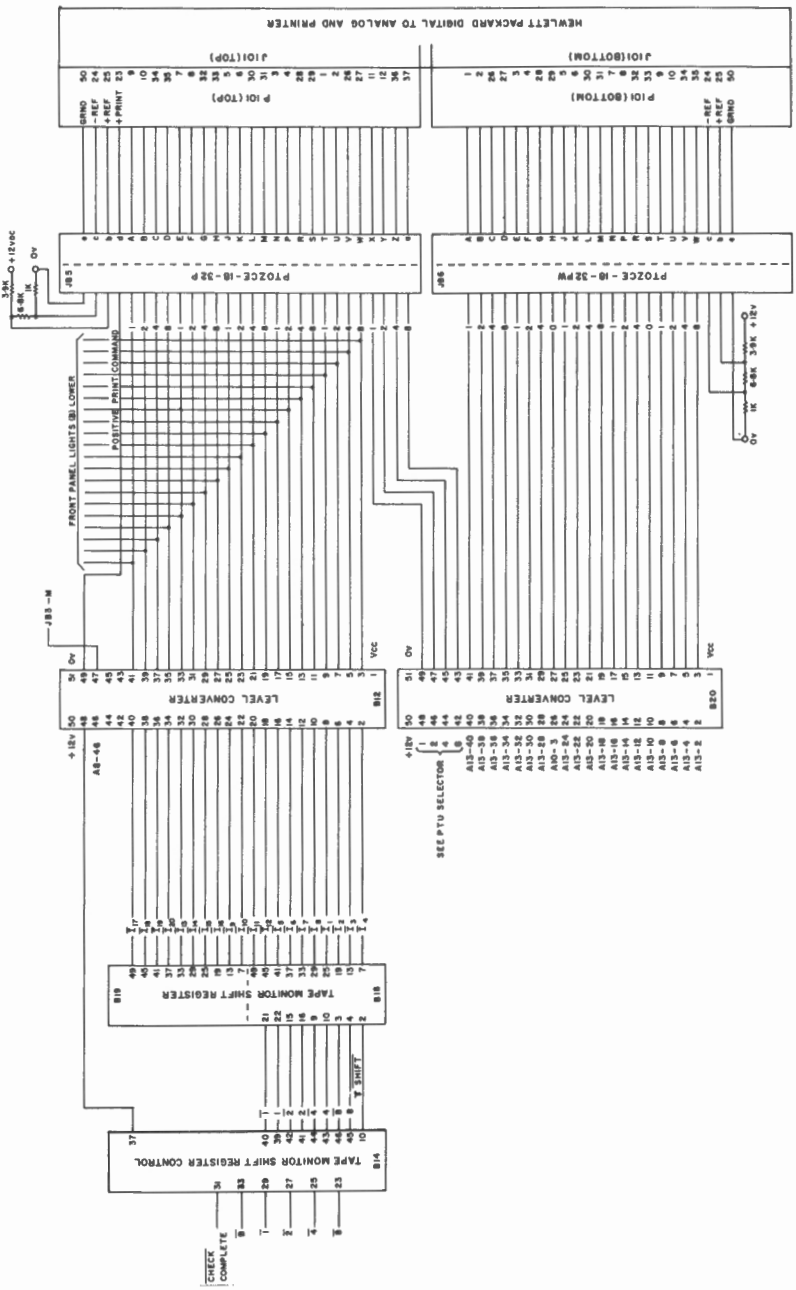


Figure 13. Time and tape monitor data to the shift register and to the digital to analog converter and printer.

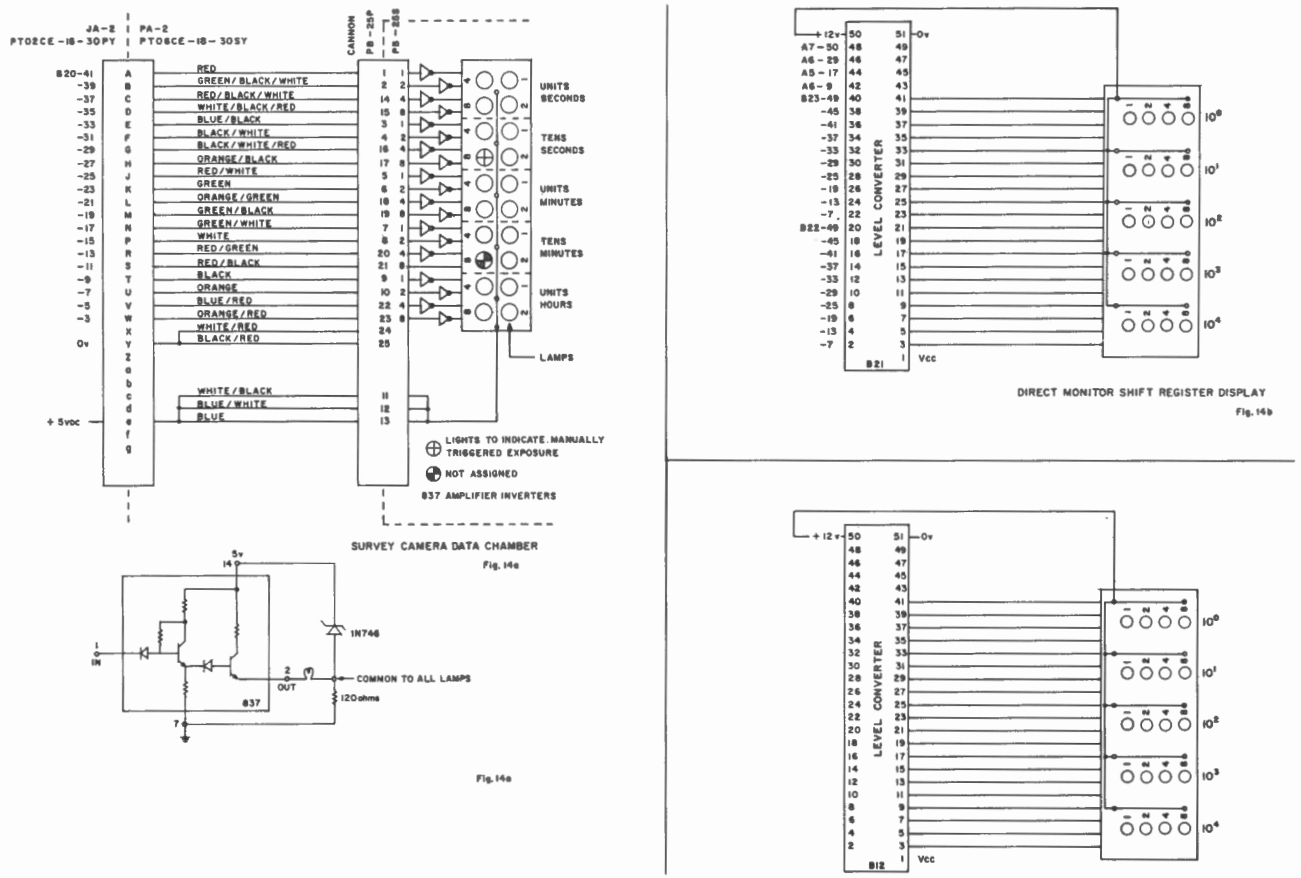


Figure 14. Time coded displays using miniature lamps for the camera data chamber, plus direct and tape monitor shift register displays.

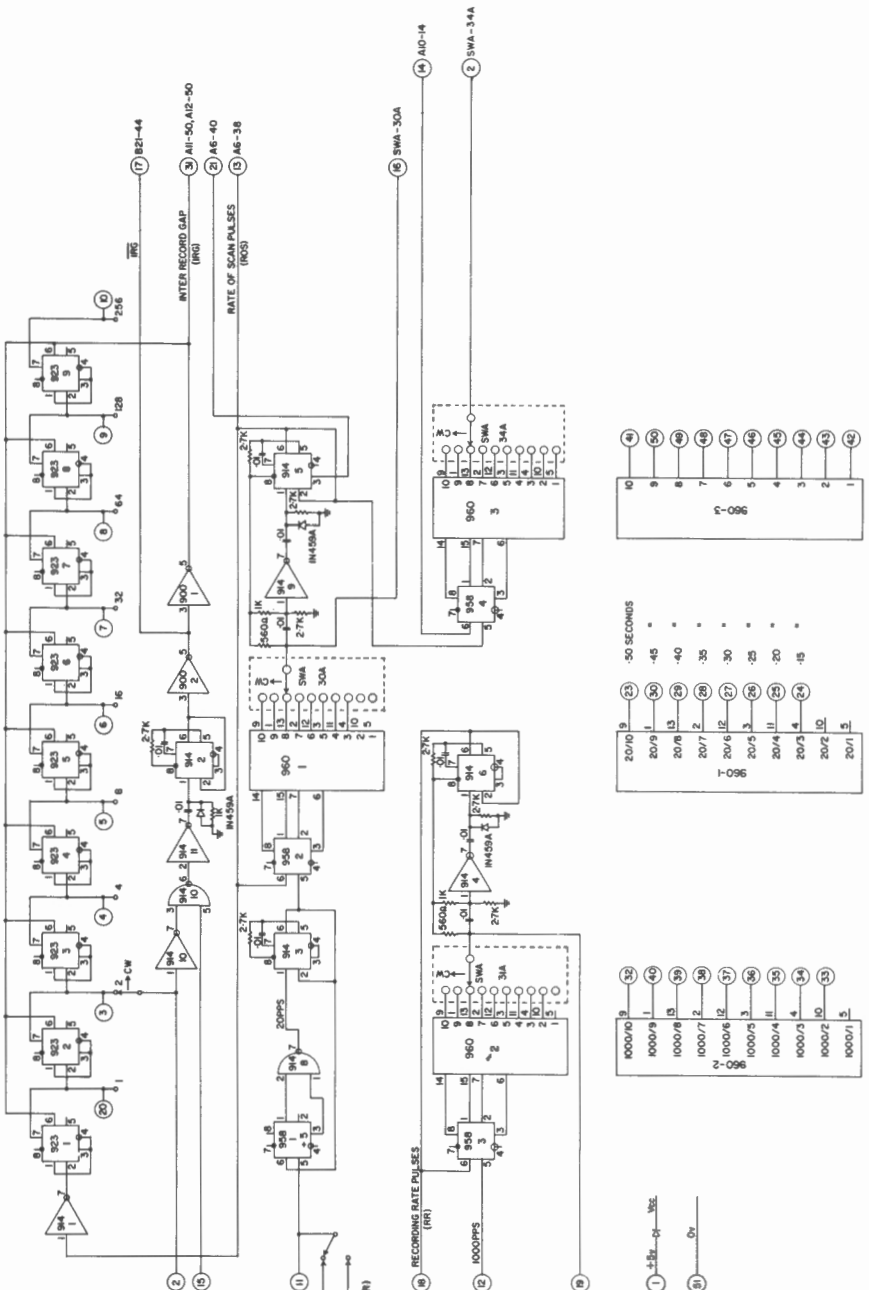


Figure 15. Master Recorder Control and interrecord gap generator.

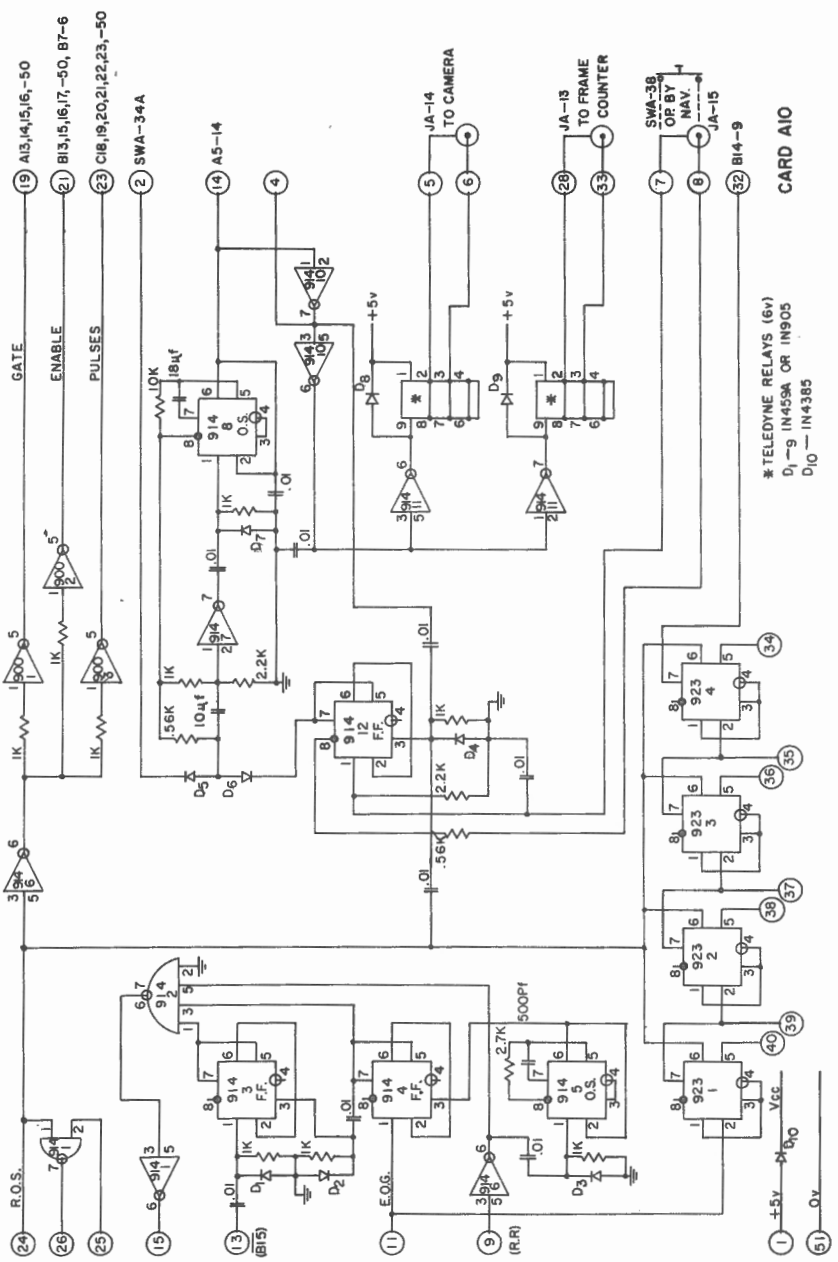


Figure 15A. Master Recorder Control Extension.

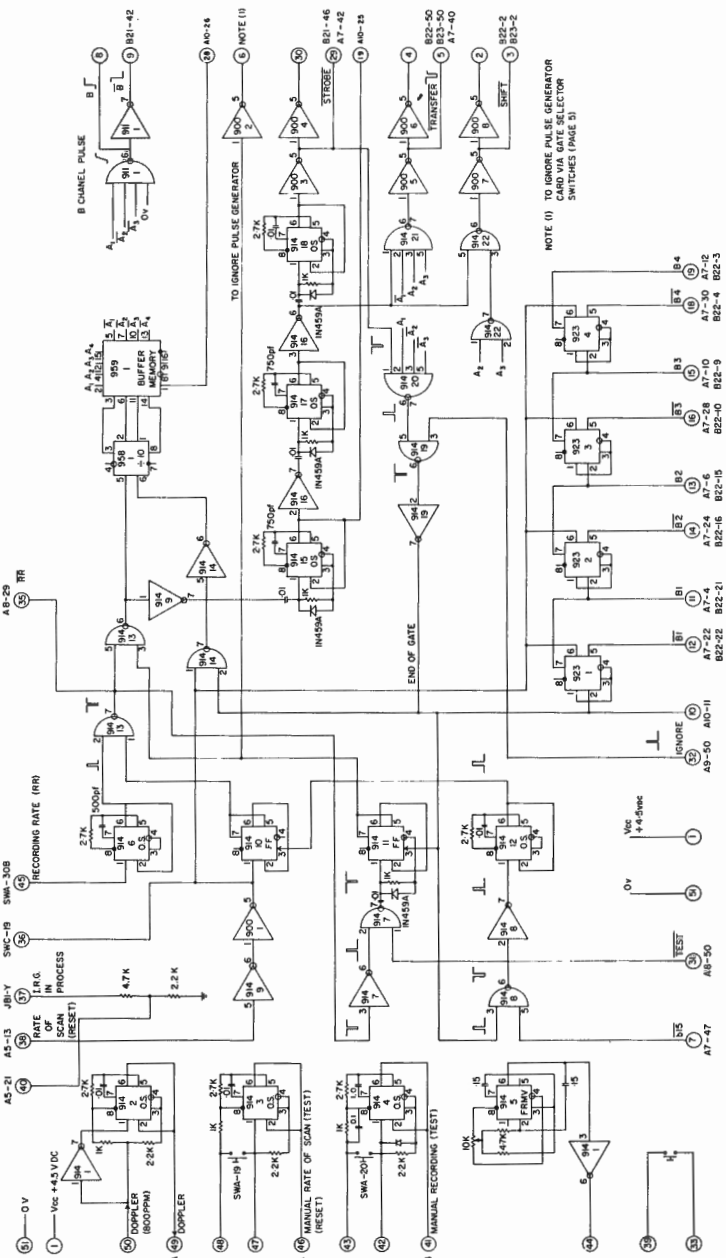


Figure 16. Magnetic tape recorder pulse sequence timer.

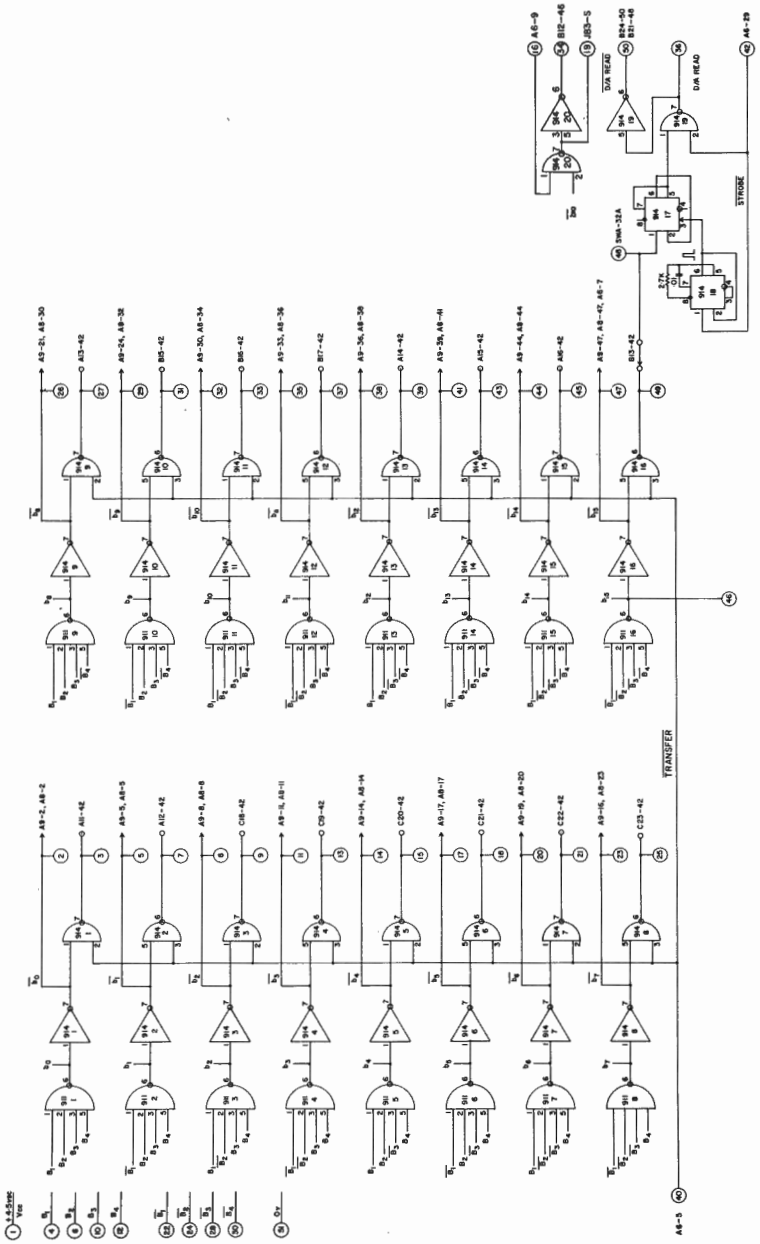


Figure 17. Master Recorder Control pulse to unit generator.

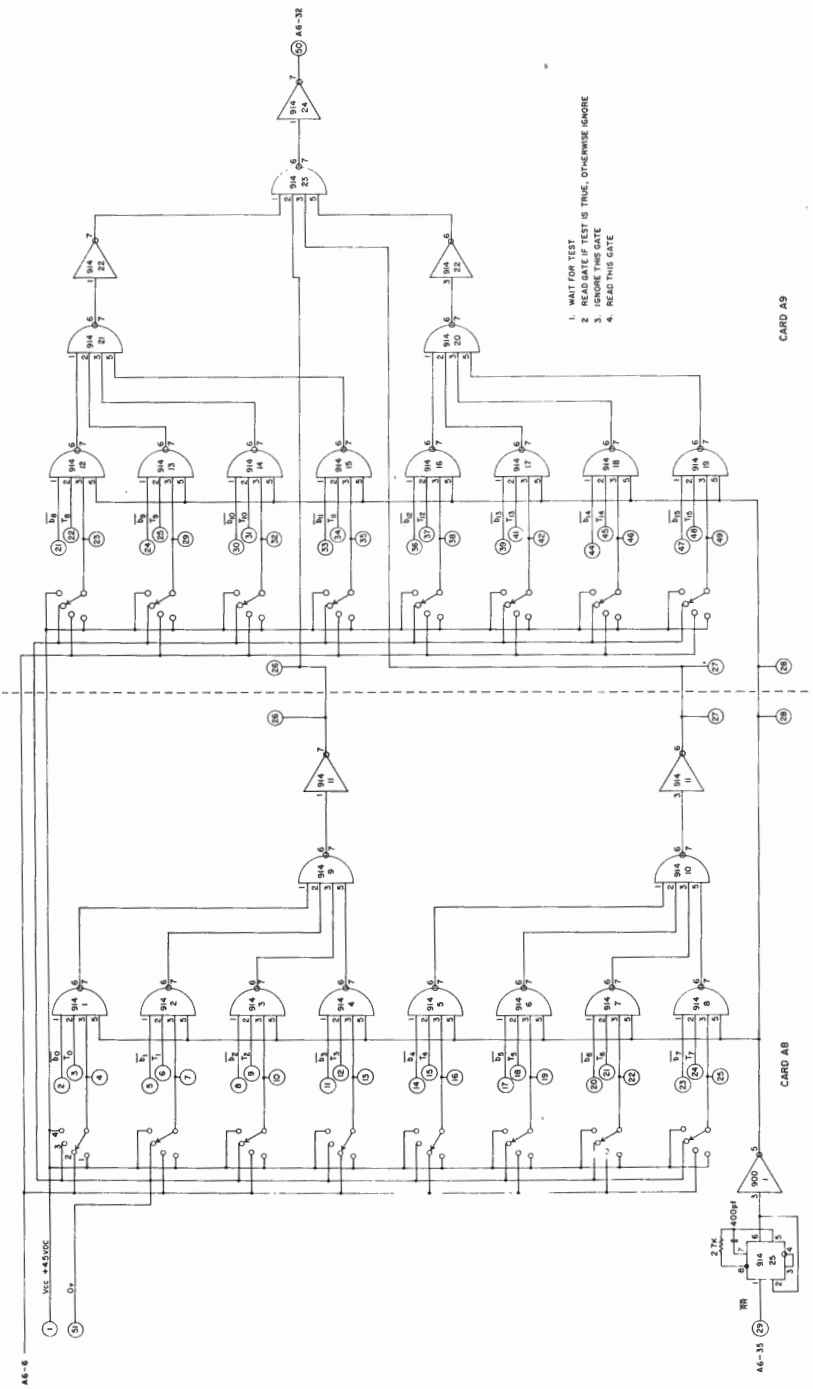


Figure 18. Master Recorder Control ignore pulse generator.

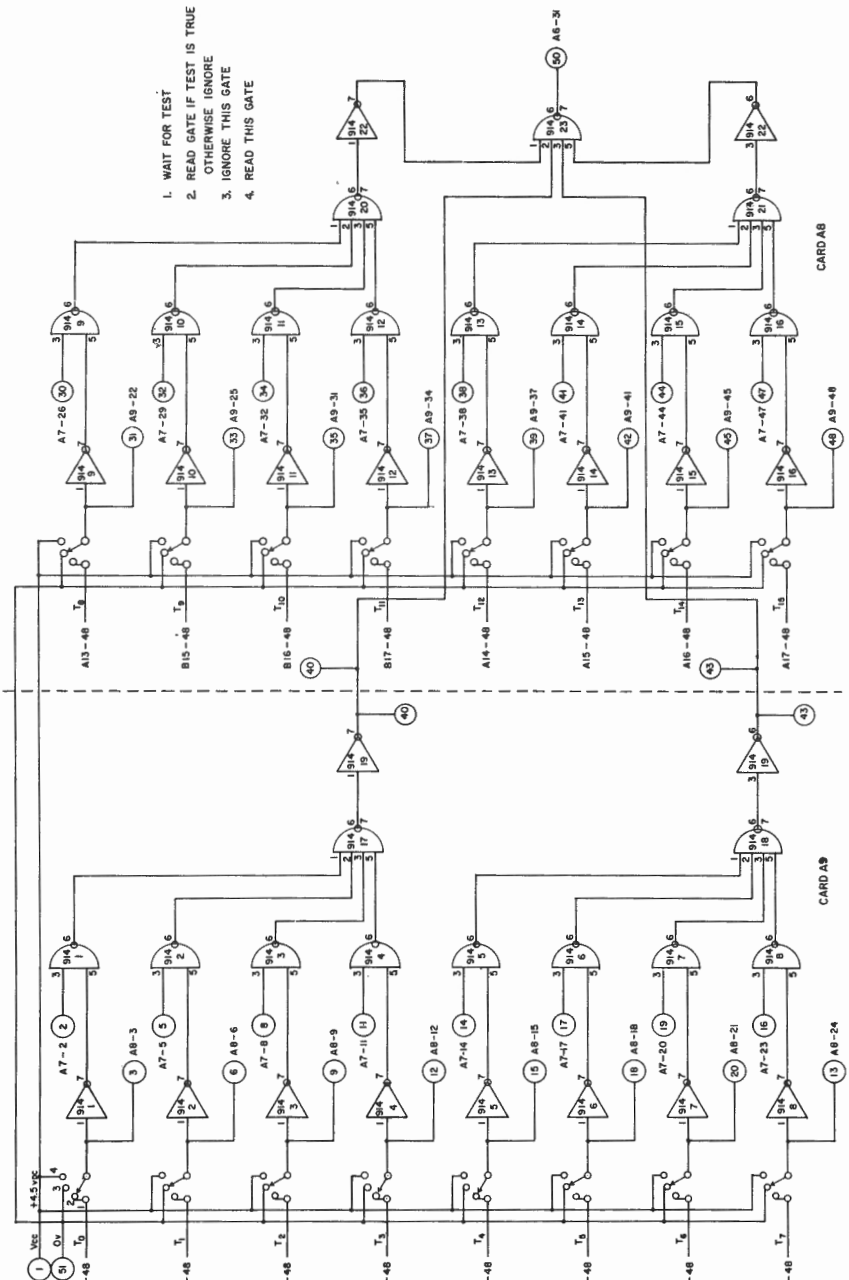


Figure 19. Master Recorder Control test pulse generator.

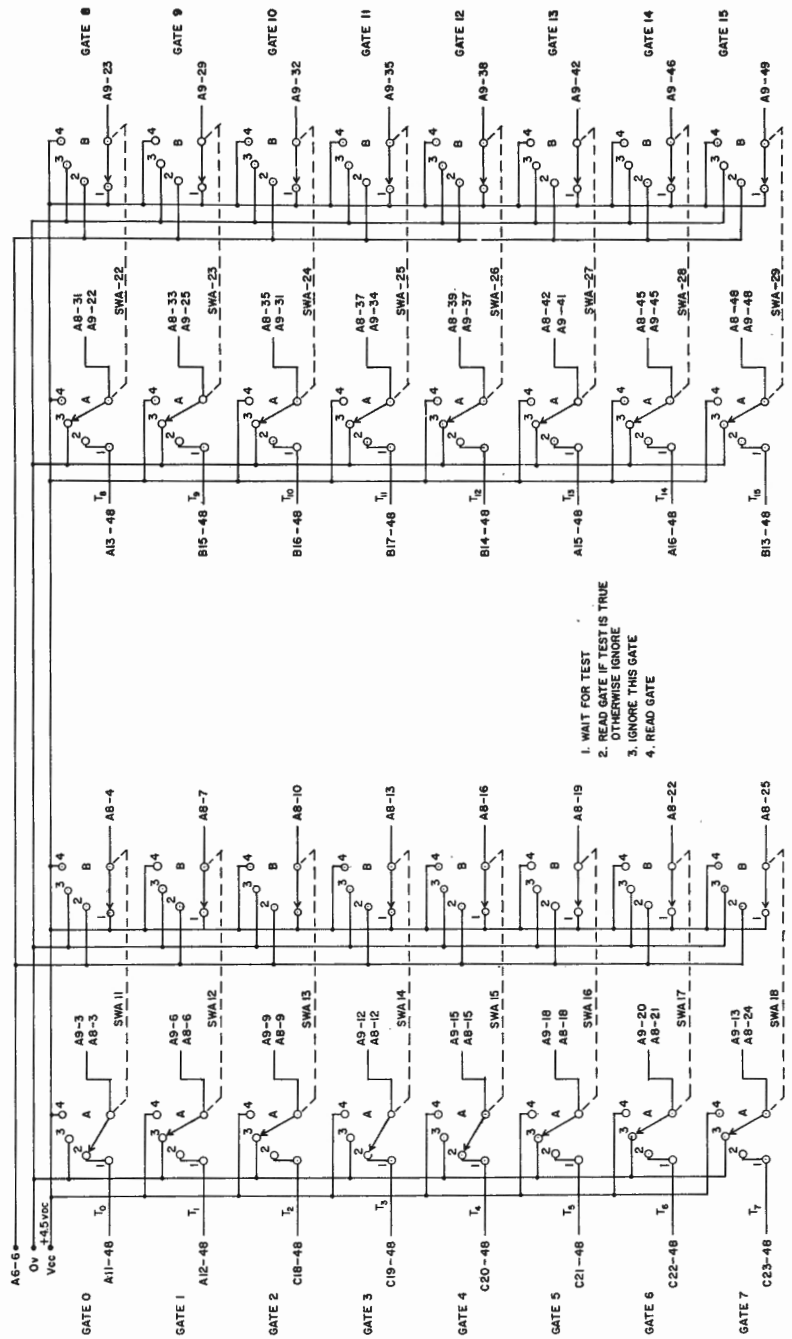


Figure 20. Interface gate selector switches.

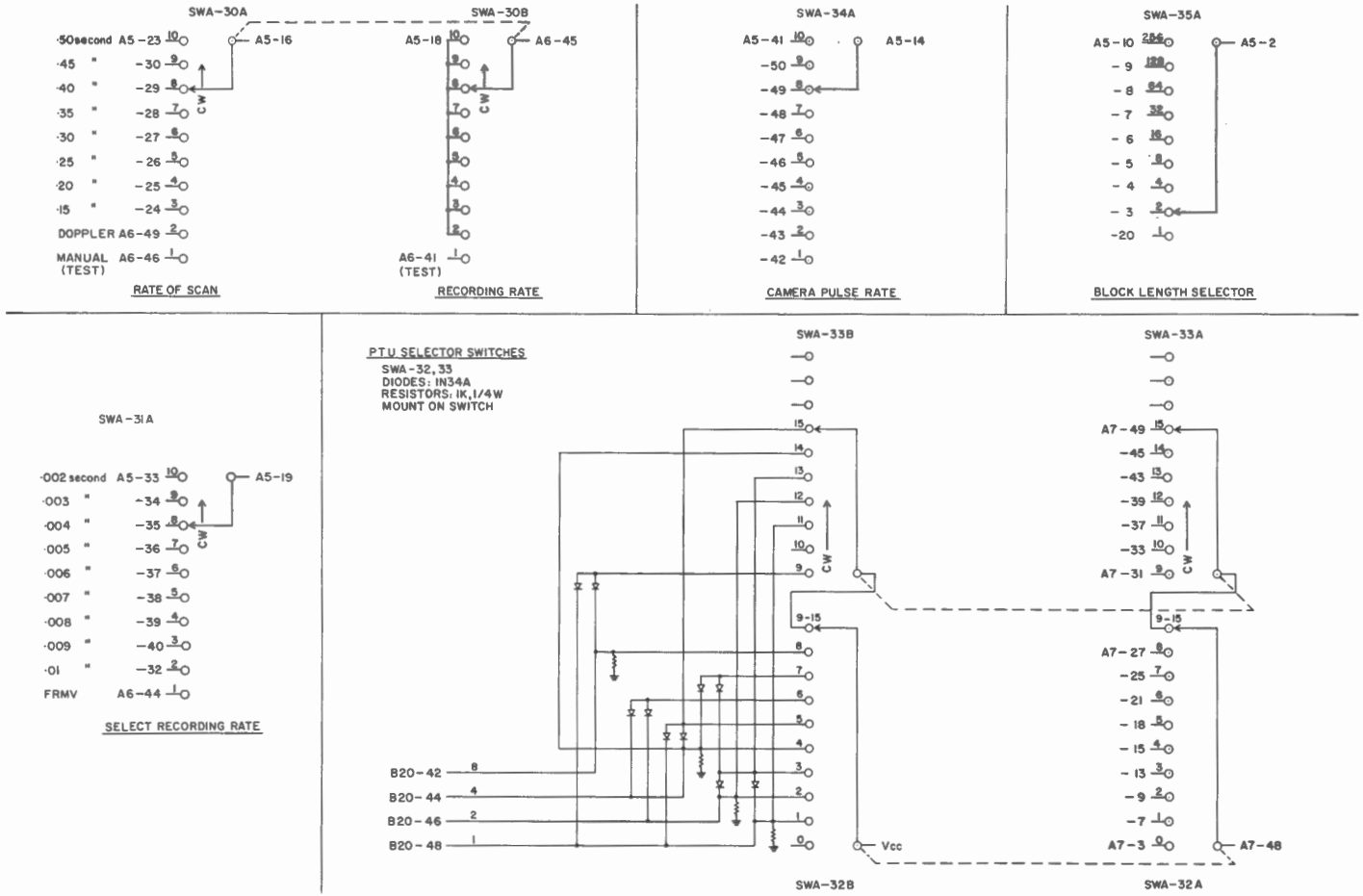


Figure 21. Rate of scan, recording rate, camera firing rate, block length selector, select recording rate and pulse to unit selector switches.

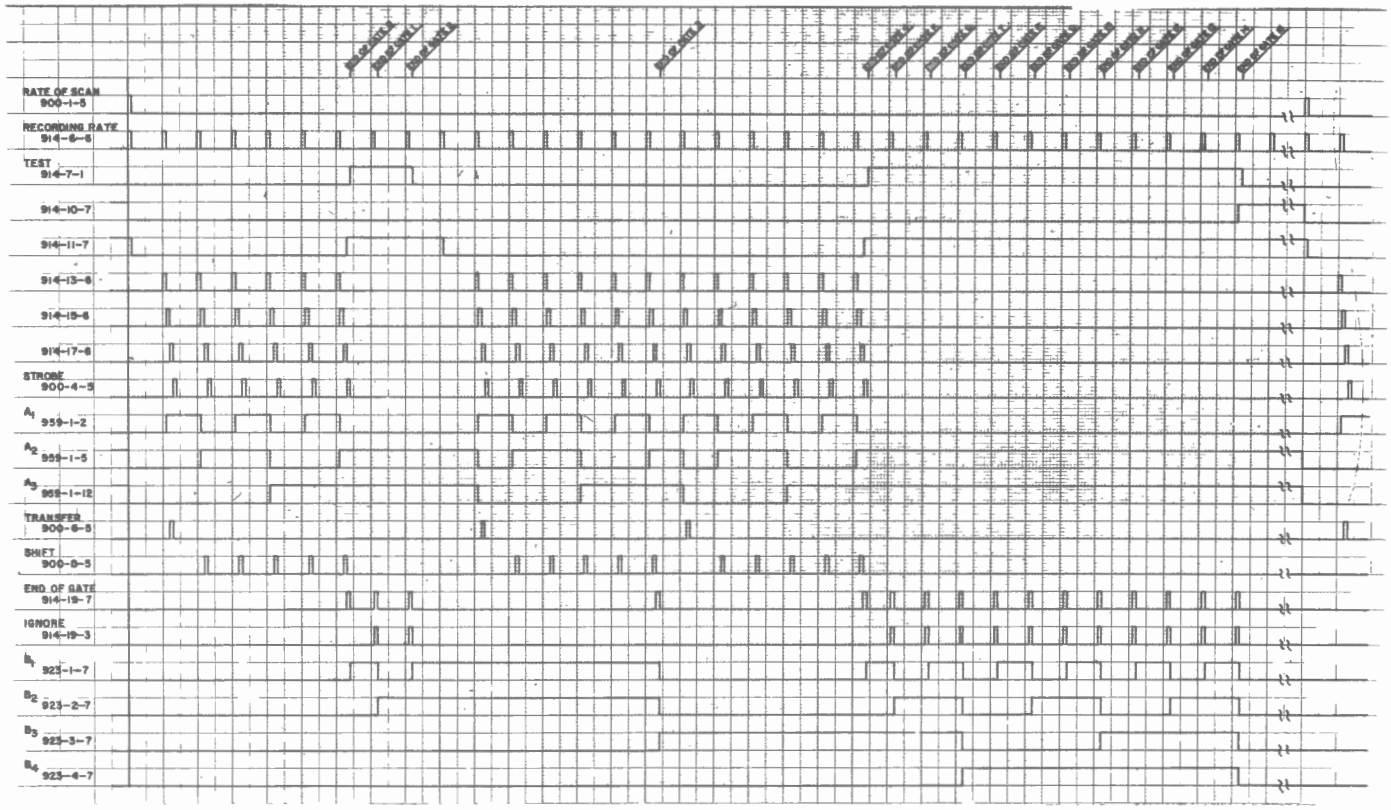


Figure 22. Master Recorder Control timing diagram.

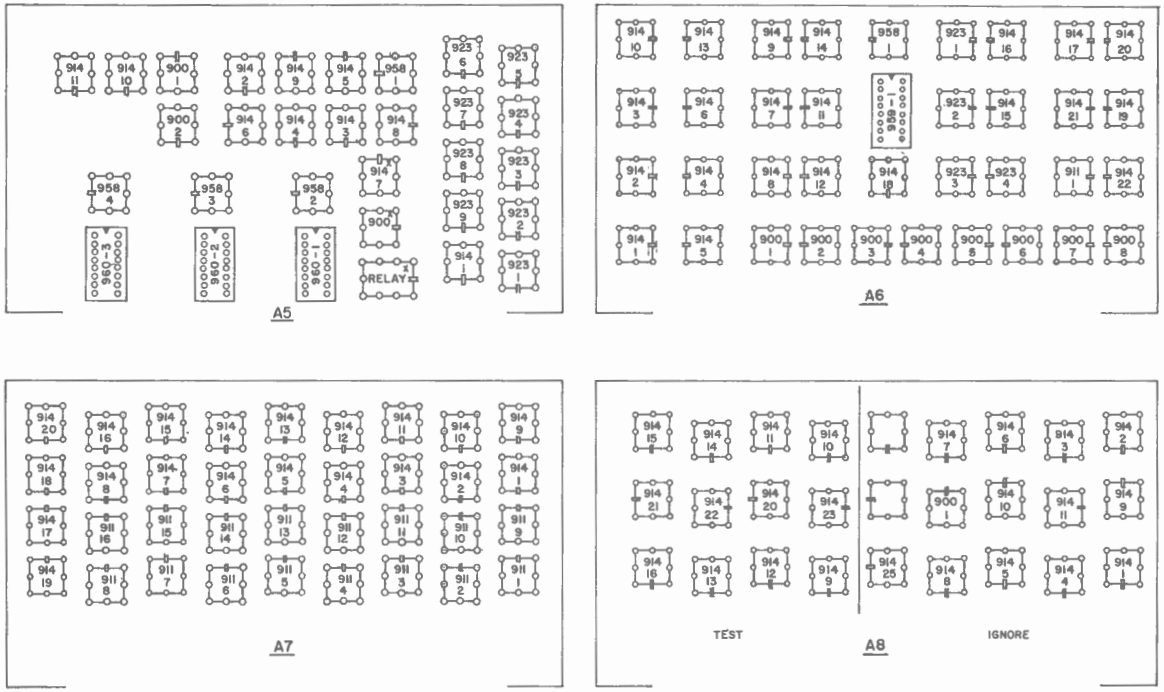
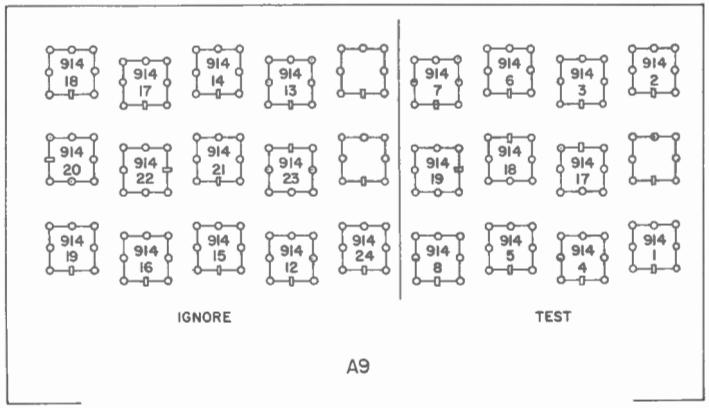
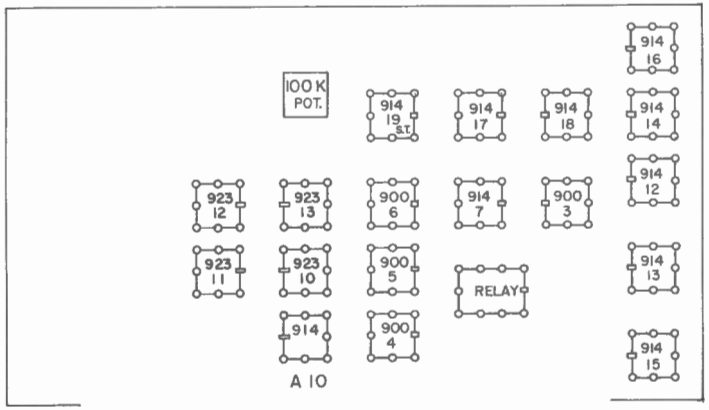


Figure 23. Master Recorder Control card layout A 5-8.





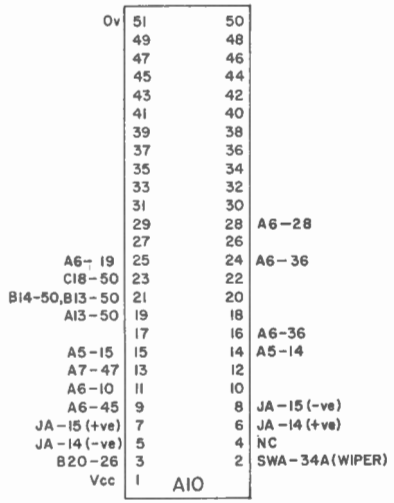


Figure 24. Master Recorder Control card layout A 9-10.

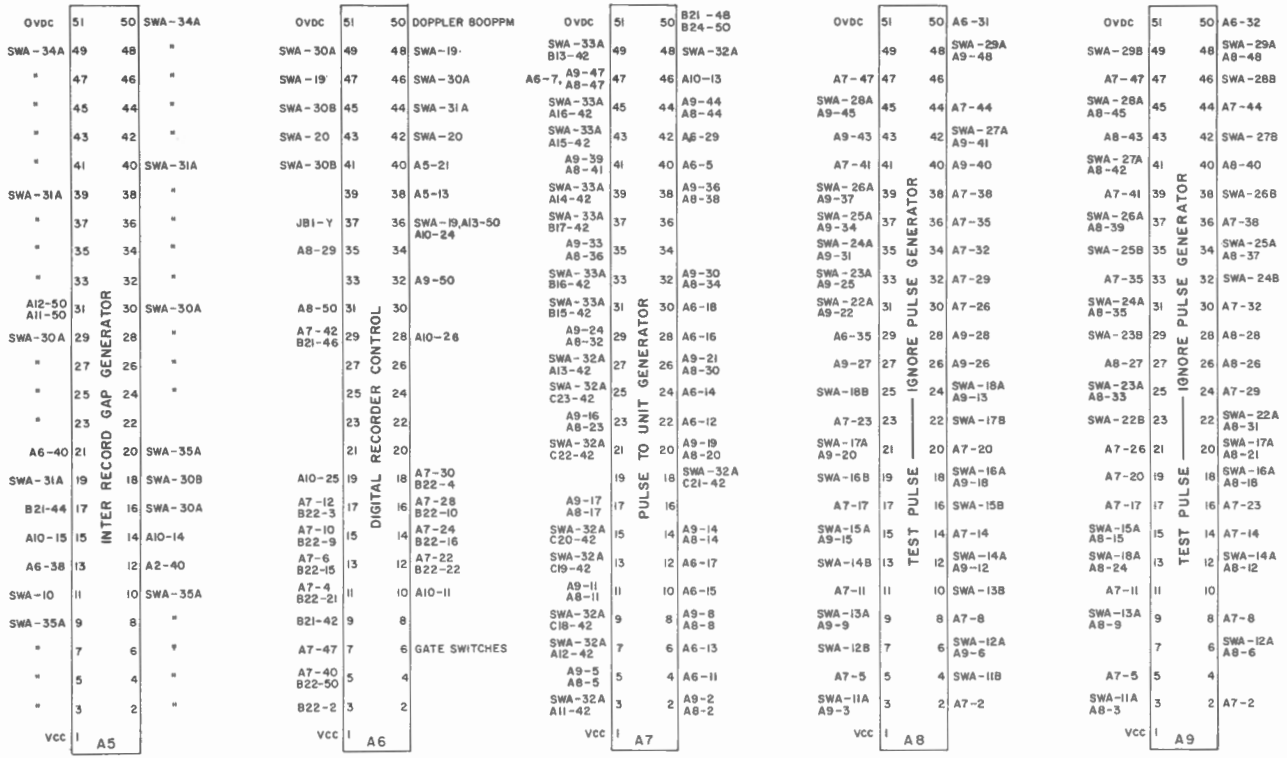


Figure 25. Master Recorder Control intercard wiring.

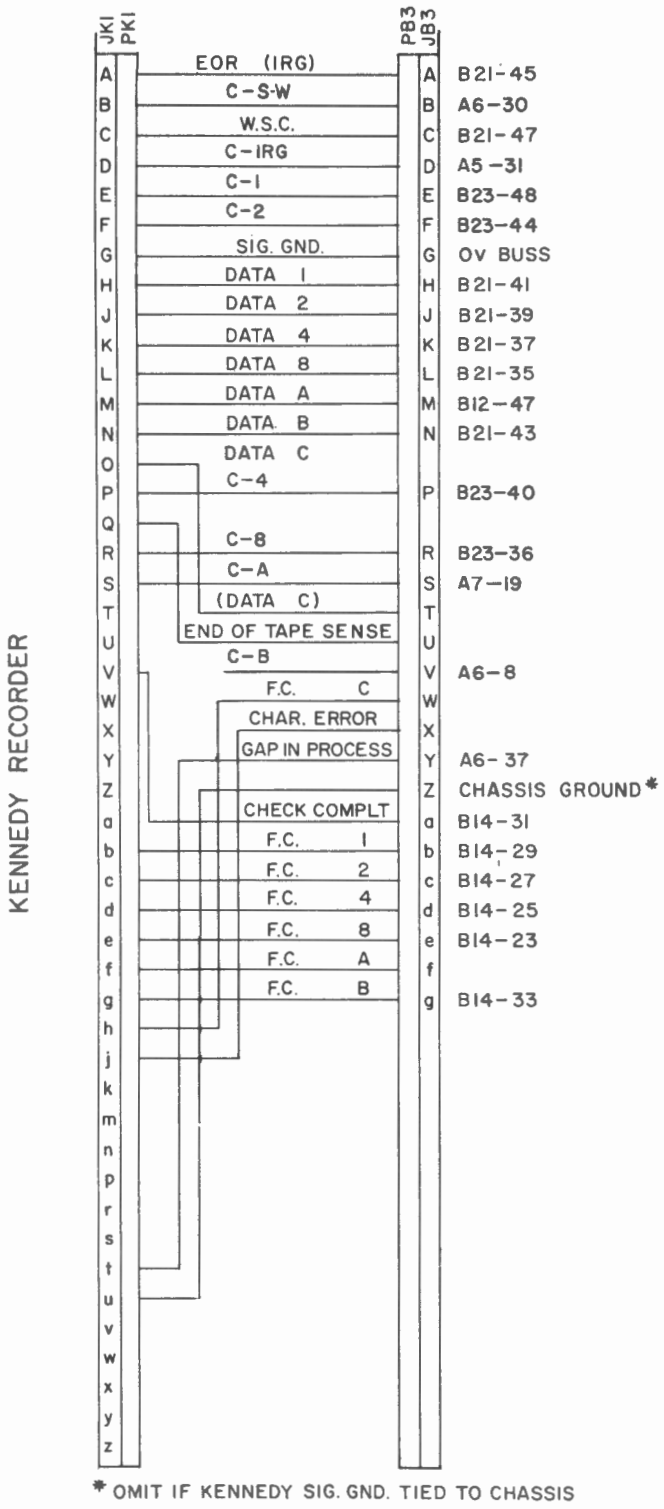
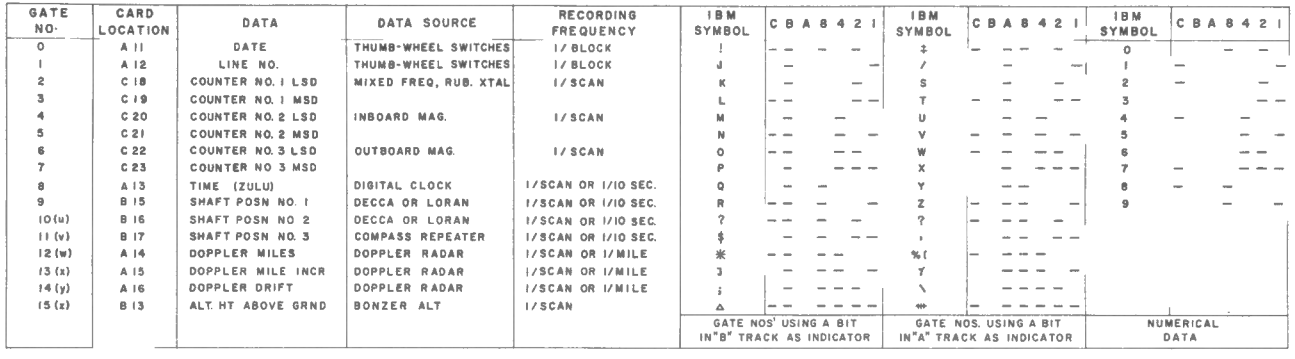


Figure 26. Kennedy digital incremental magnetic tape recorder cabling diagram.



GATE NO.	CARD LOCATION	DATA	DATA SOURCE	RECORDING FREQUENCY	IBM SYMBOL	C B A 8 4 2 1	IBM SYMBOL	C B A 8 4 2 1	IBM SYMBOL	C B A 8 4 2 1
0	A 11	DATE	THUMB-WHEEL SWITCHES	1/BLOCK	!	– – – – –	‡	– – – – –	0	– –
1	A 12	LINE NO.	THUMB-WHEEL SWITCHES	1/BLOCK	J	– – –	/	– – –	1	– –
2	C 18	COUNTER NO. 1 LSD	MIXED FREQ, RUB. XTAL	1/SCAN	K	– – –	S	– – –	2	– –
3	C 19	COUNTER NO. 1 MSD			L	– – – –	T	– – – –	3	– –
4	C 20	COUNTER NO. 2 LSD	INBOARD MAG.	1/SCAN	M	– – –	U	– – –	4	– –
5	C 21	COUNTER NO. 2 MSD			N	– – – –	V	– – – –	5	– –
6	C 22	COUNTER NO. 3 LSD	OUTBOARD MAG.	1/SCAN	O	– – – –	W	– – – –	6	– –
7	C 23	COUNTER NO 3 MSD			P	– – – – –	X	– – – – –	7	– – –
8	A 13	TIME (ZULU)	DIGITAL CLOCK	1/SCAN OR 1/10 SEC.	Q	– – –	Y	– – –	8	– –
9	B 15	SHAFT POSN NO. 1	DECCA OR LORAN	1/SCAN OR 1/10 SEC.	R	– – – –	Z	– – – –	9	– –
10(u)	B 16	SHAFT POSN NO 2	DECCA OR LORAN	1/SCAN OR 1/10 SEC.	?	– – – –	?	– – – –		
11(v)	B 17	SHAFT POSN NO. 3	COMPASS REPEATER	1/SCAN OR 1/10 SEC.	$	– – – –	,	– – – –		
12(w)	A 14	DOPPLER MILES	DOPPLER RADAR	1/SCAN OR 1/MILE	*	– – – –	%(	– – – –		
13(x)	A 15	DOPPLER MILE INCR	DOPPLER RADAR	1/SCAN OR 1/MILE	]	– – – –	'	– – – – –		
14(y)	A 16	DOPPLER DRIFT	DOPPLER RADAR	1/SCAN OR 1/MILE	;	– – – –	\	– – – –		
15(z)	B 13	ALT. HT ABOVE GRND	BONZER ALT	1/SCAN	Δ	– – – – – –	⇔	– – – – – –		
					GATE NOS' USING A BIT IN "B" TRACK AS INDICATOR		GATE NOS. USING A BIT IN "A" TRACK AS INDICATOR		NUMERICAL DATA	

Figure 27. Data and gate number code using IBM interchange code.

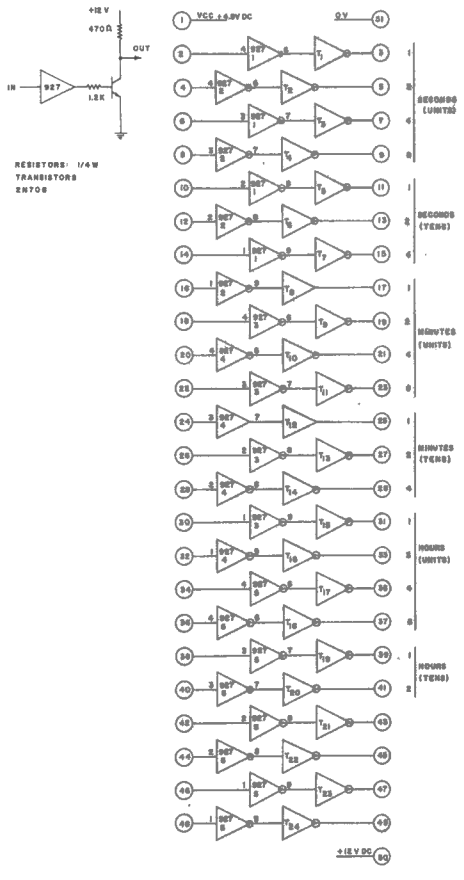
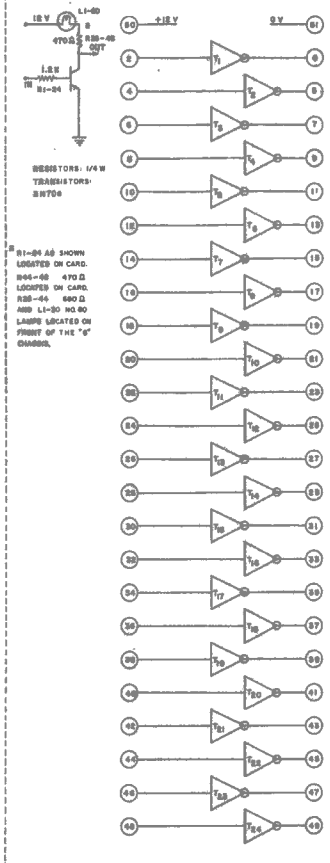
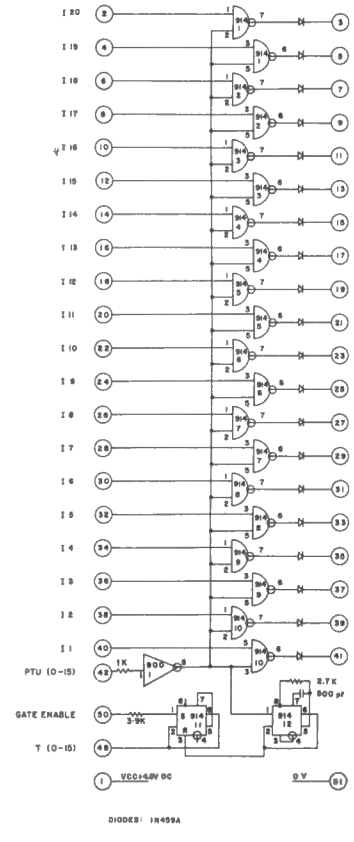


Figure 28A. Diagram of the level converter.



28B. Diagram of the double inversion level converter.



28C. Diagram of the interface gate card.

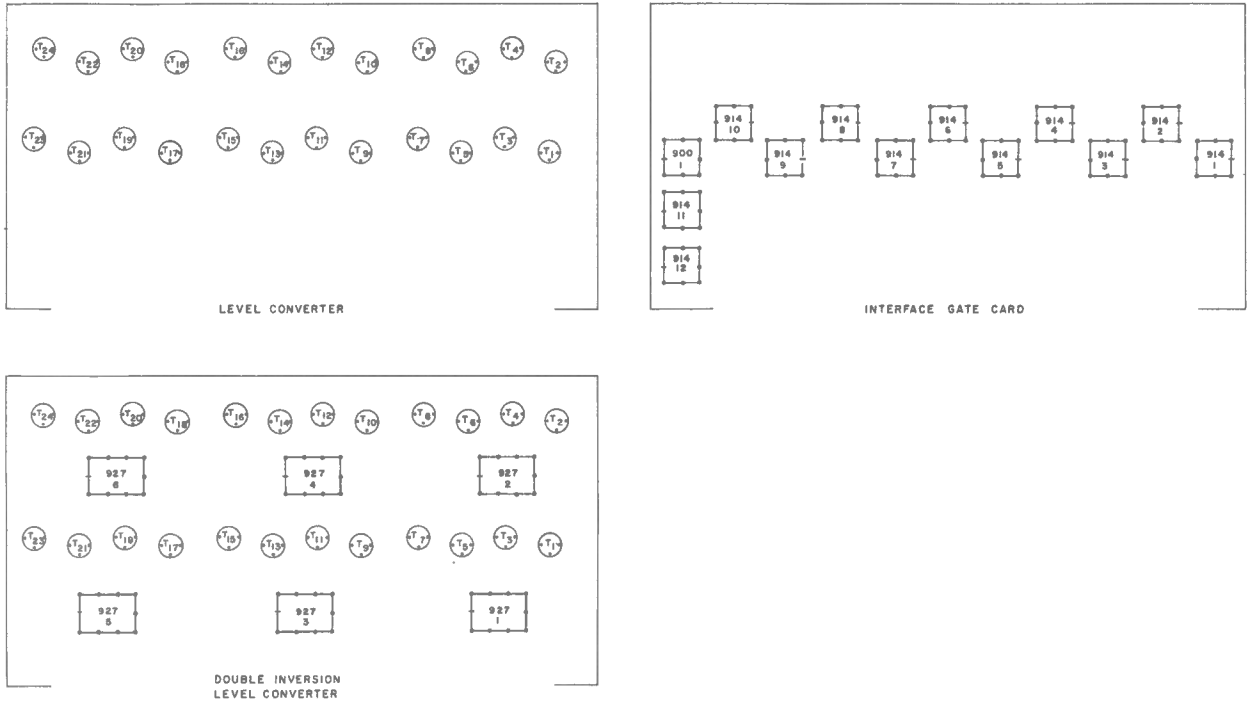


Figure 29. Interface gate card and level converter card layout.

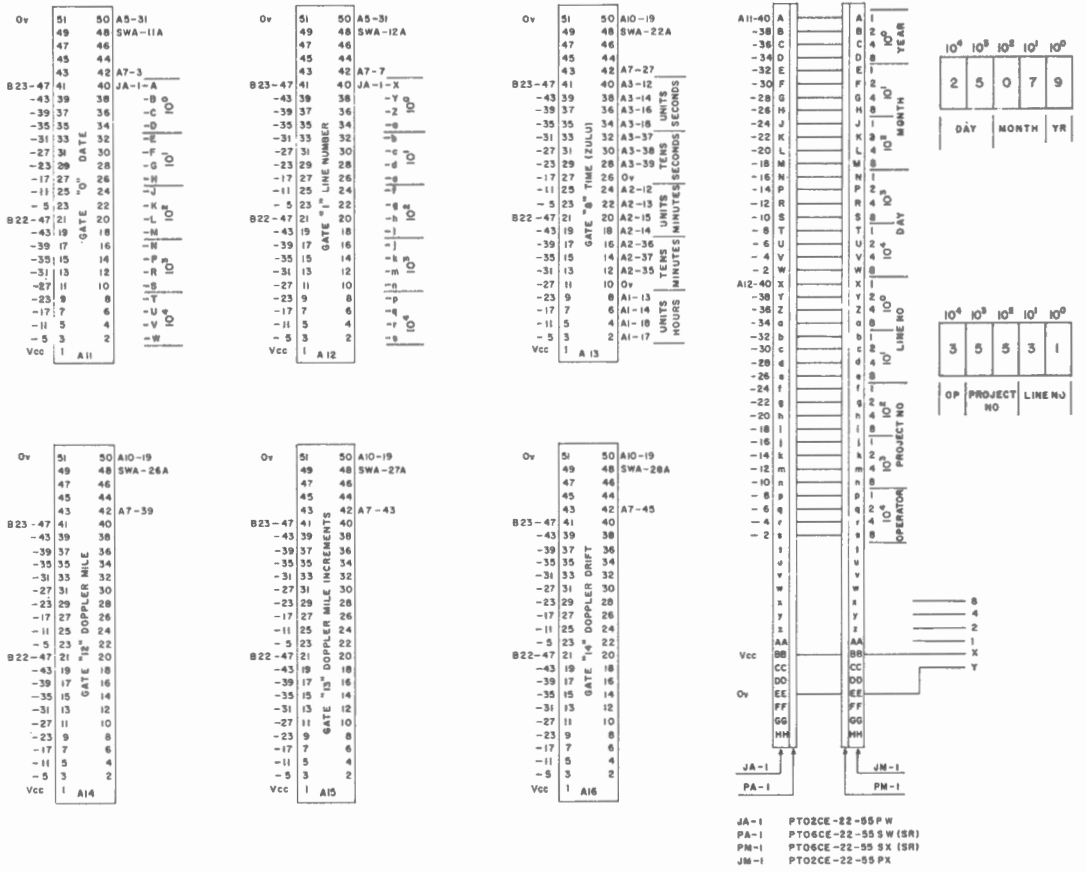


Figure 30. Intercard wiring of the A chassis gate cards.

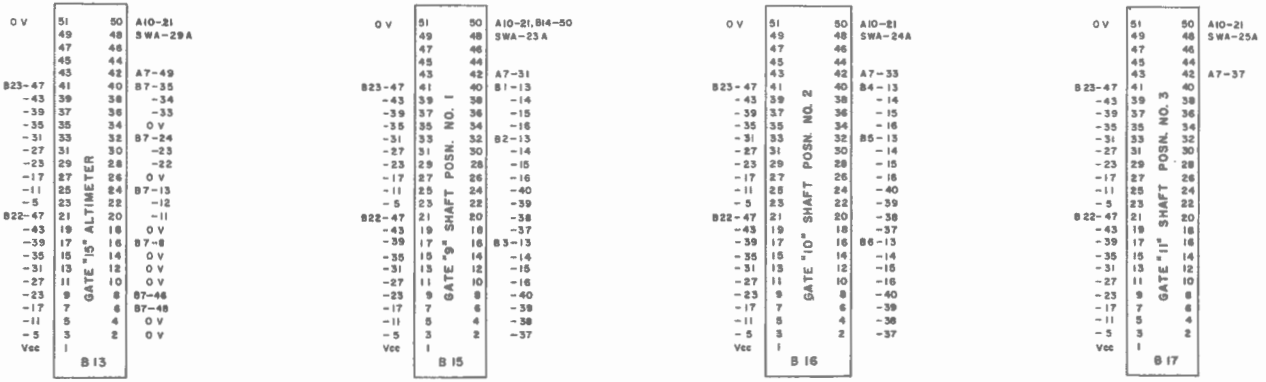


Figure 31. Intercard wiring of the B chassis gate cards.

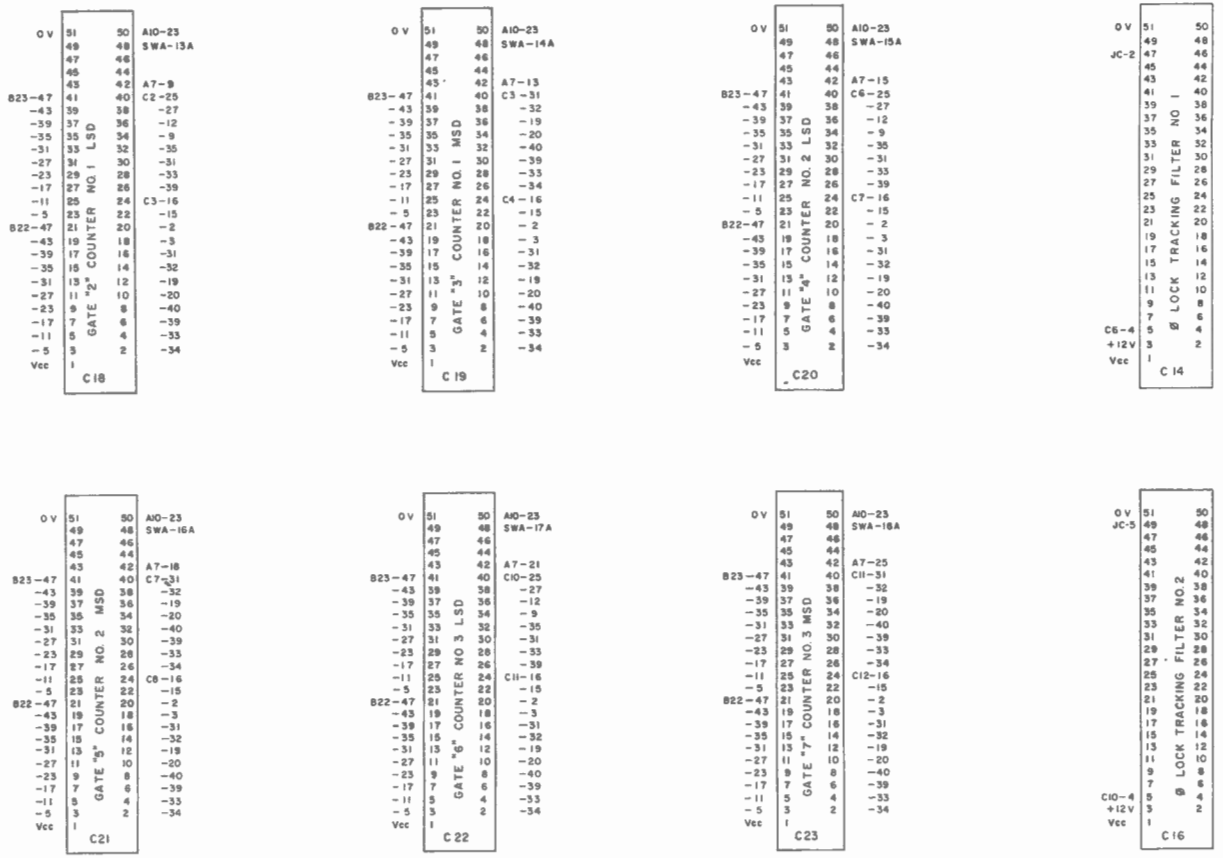


Figure 32. Intercard wiring of the C chassis gate cards.

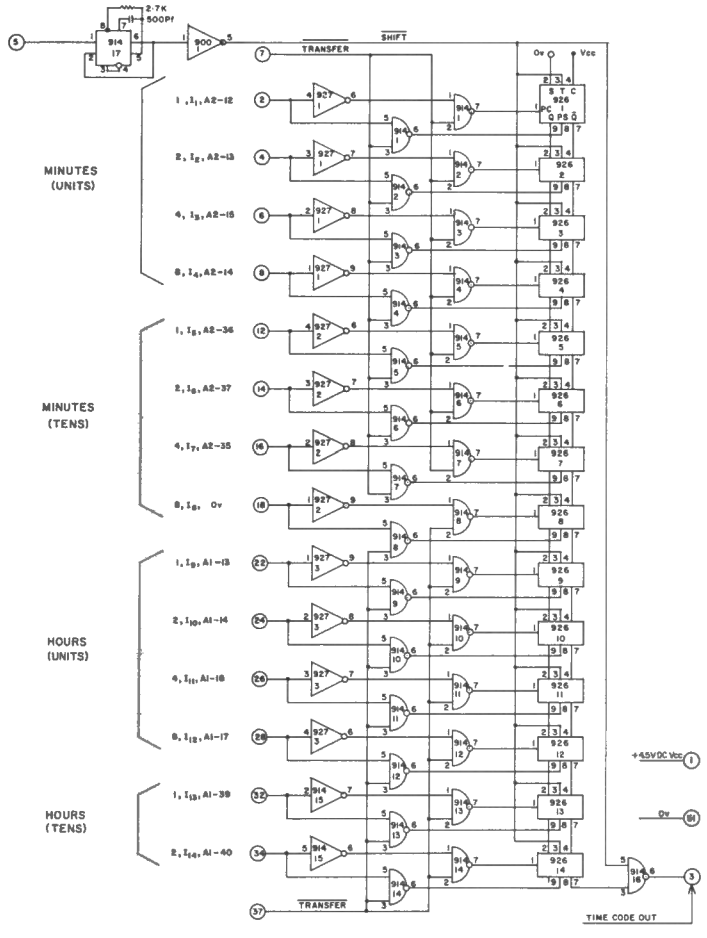
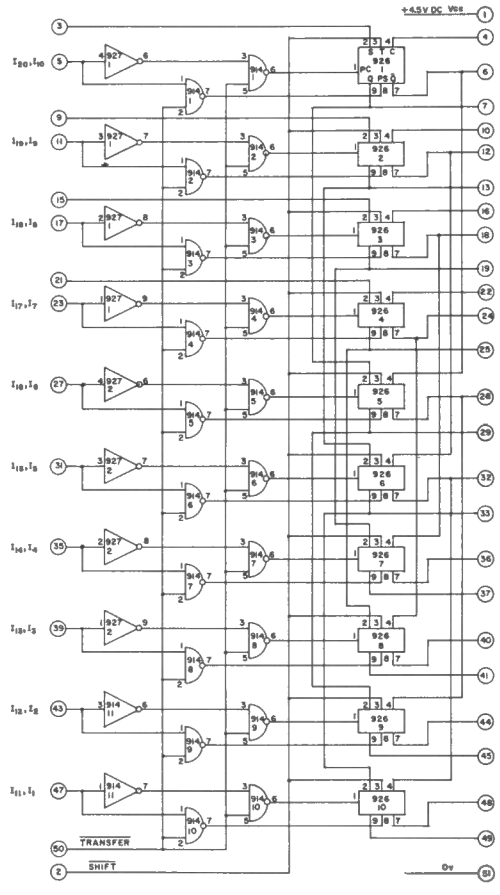


Figure 33. The Time code shift register.



The Data shift register.

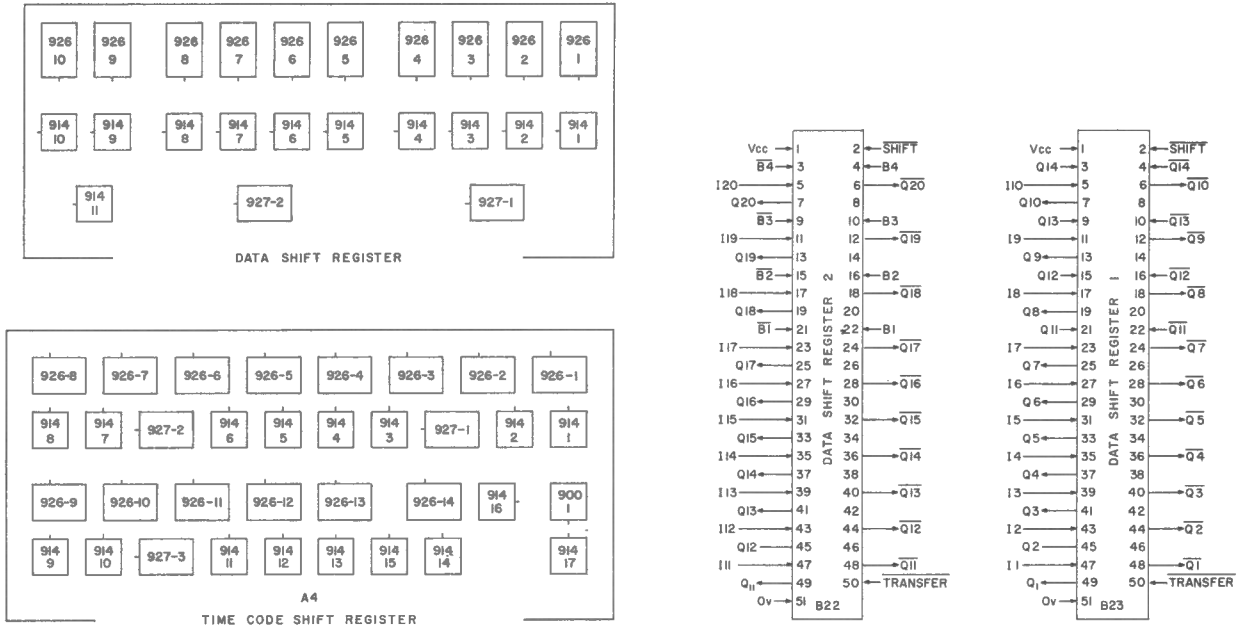


Figure 34. The shift register card layout.

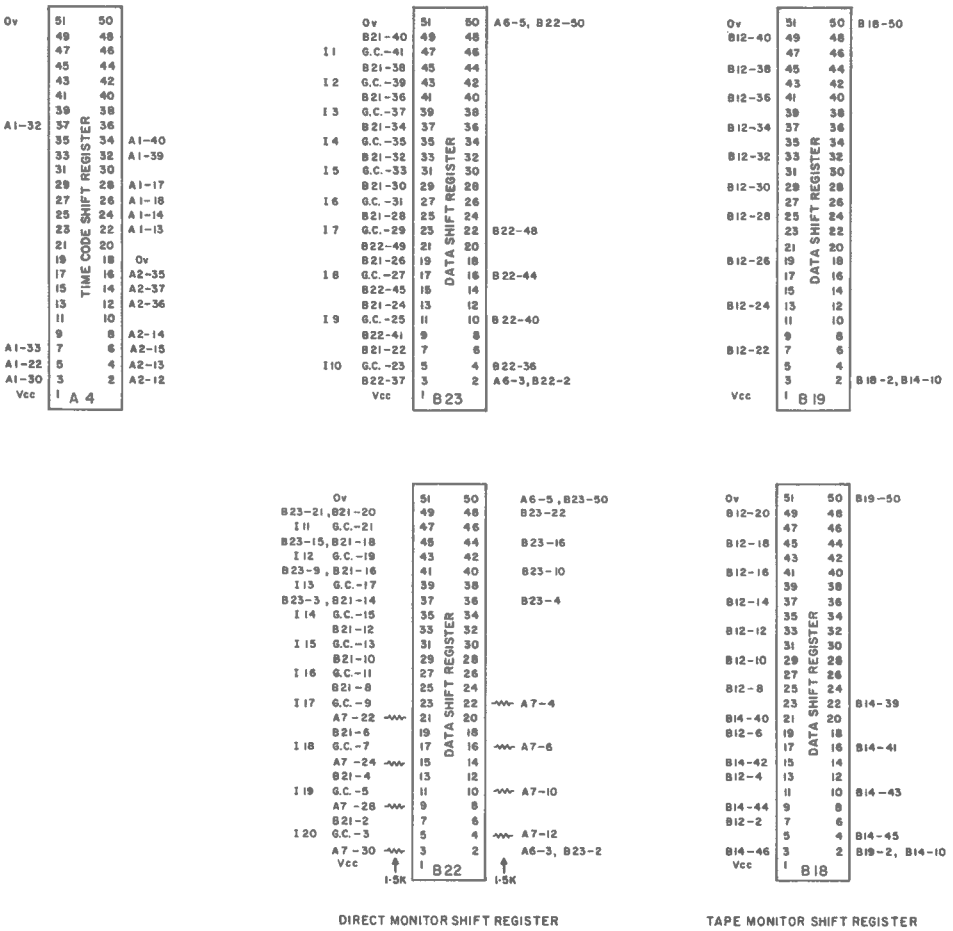


Figure 35. The shift register intercard wiring.

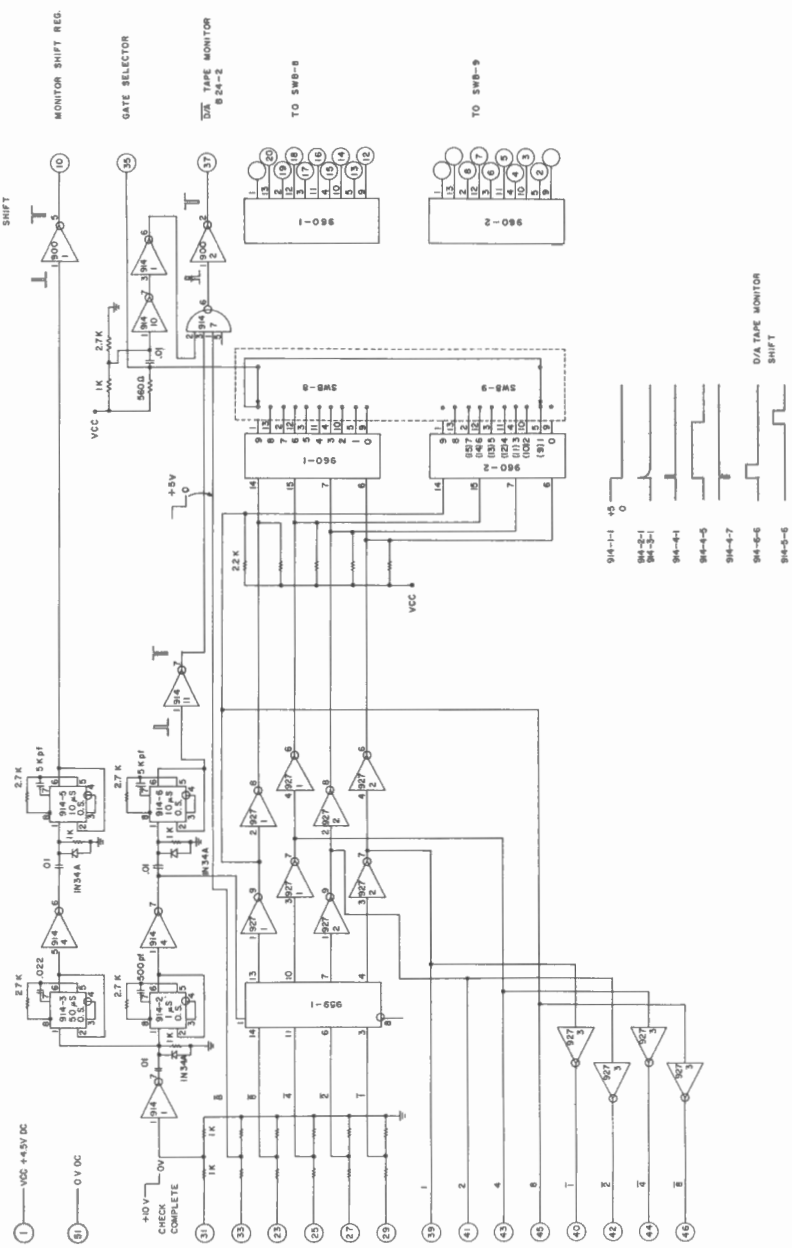


Figure 36. Tape monitor shift register control and logic diagram.

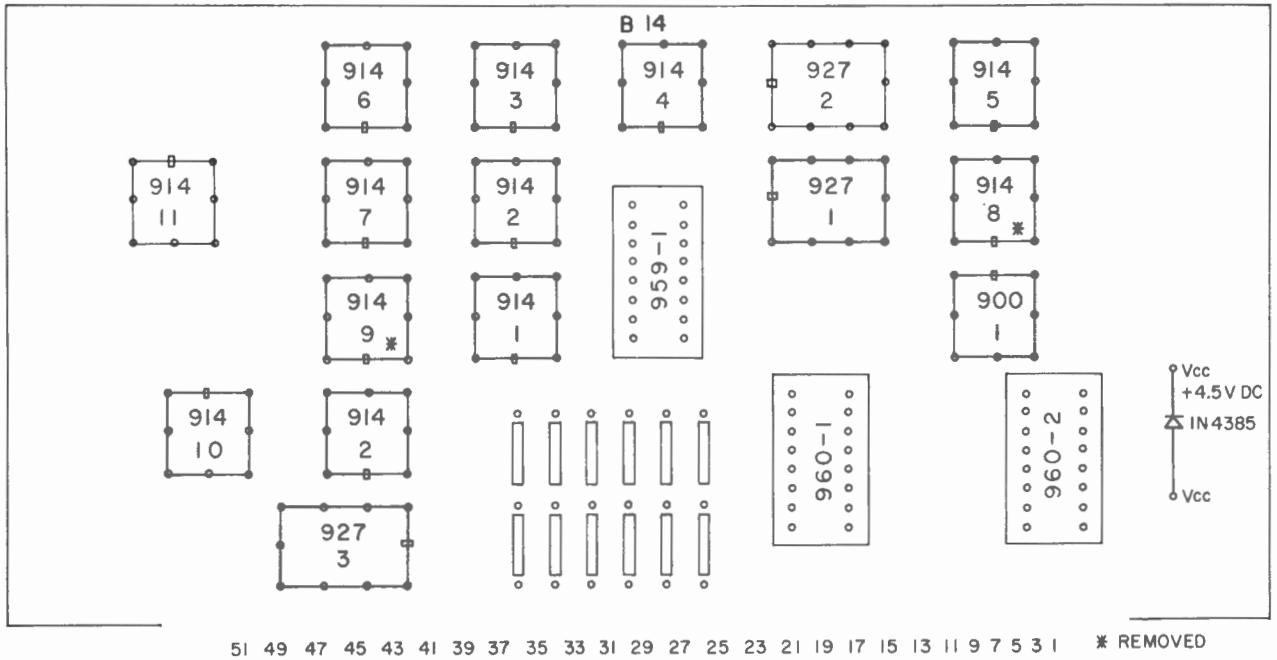


Figure 37. Tape monitor shift register control card layout.

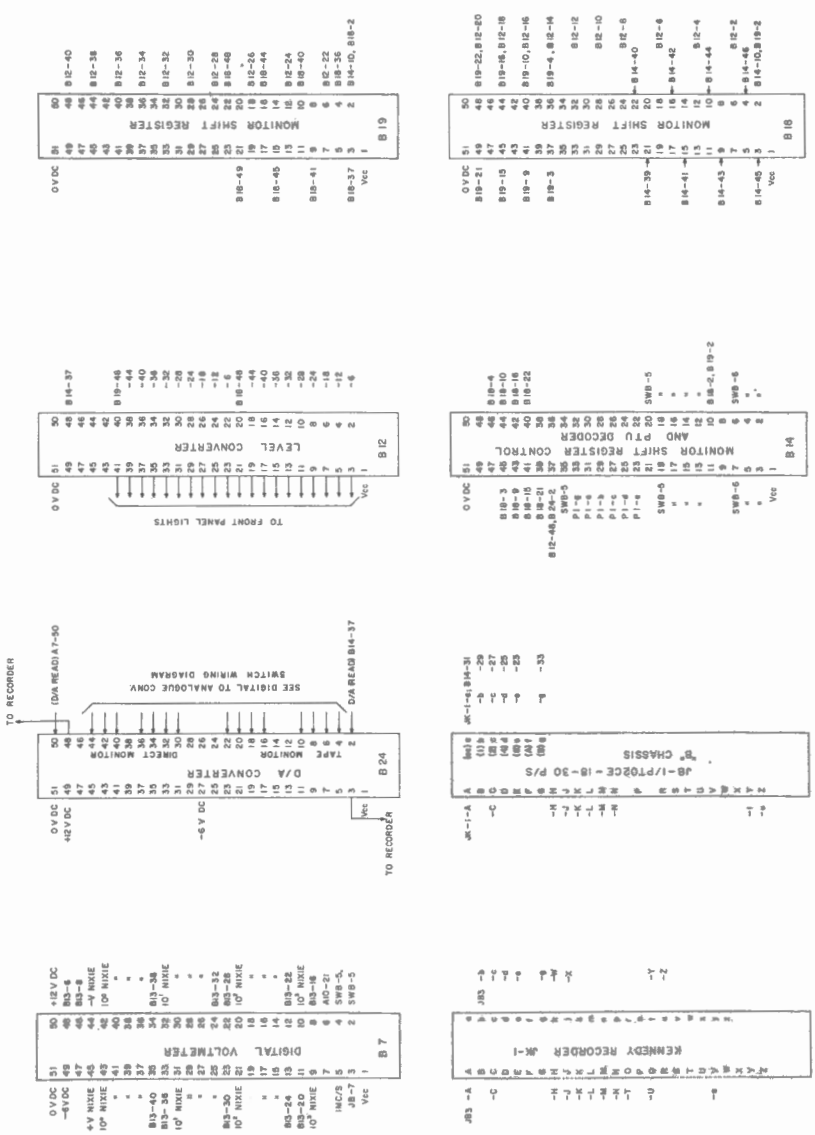


Figure 38. Tape monitor shift register control intercard wiring.

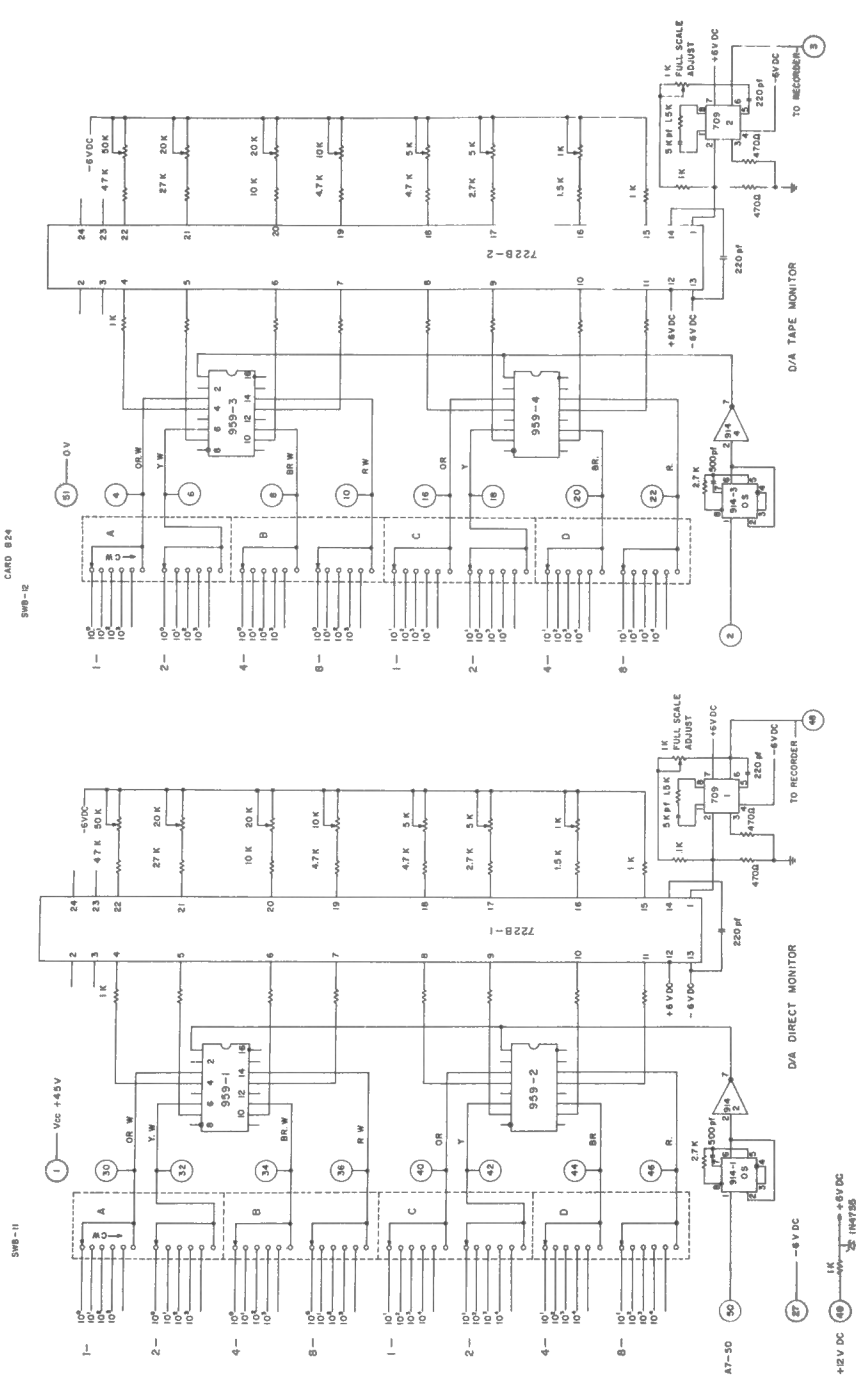


Figure 39. The digital to analog converter logic diagram.

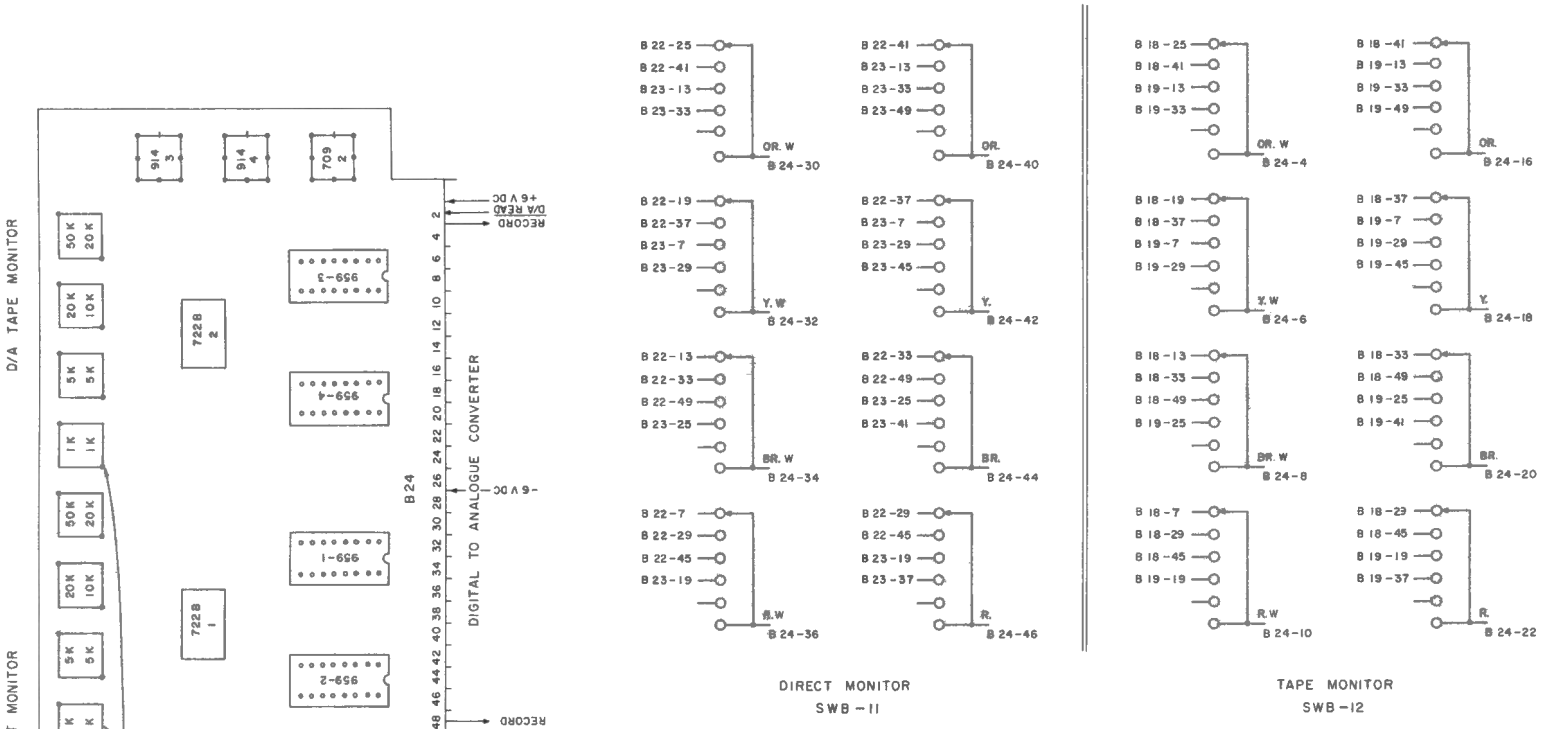


Figure 40. The digital to analog converter card layout and switching diagram.

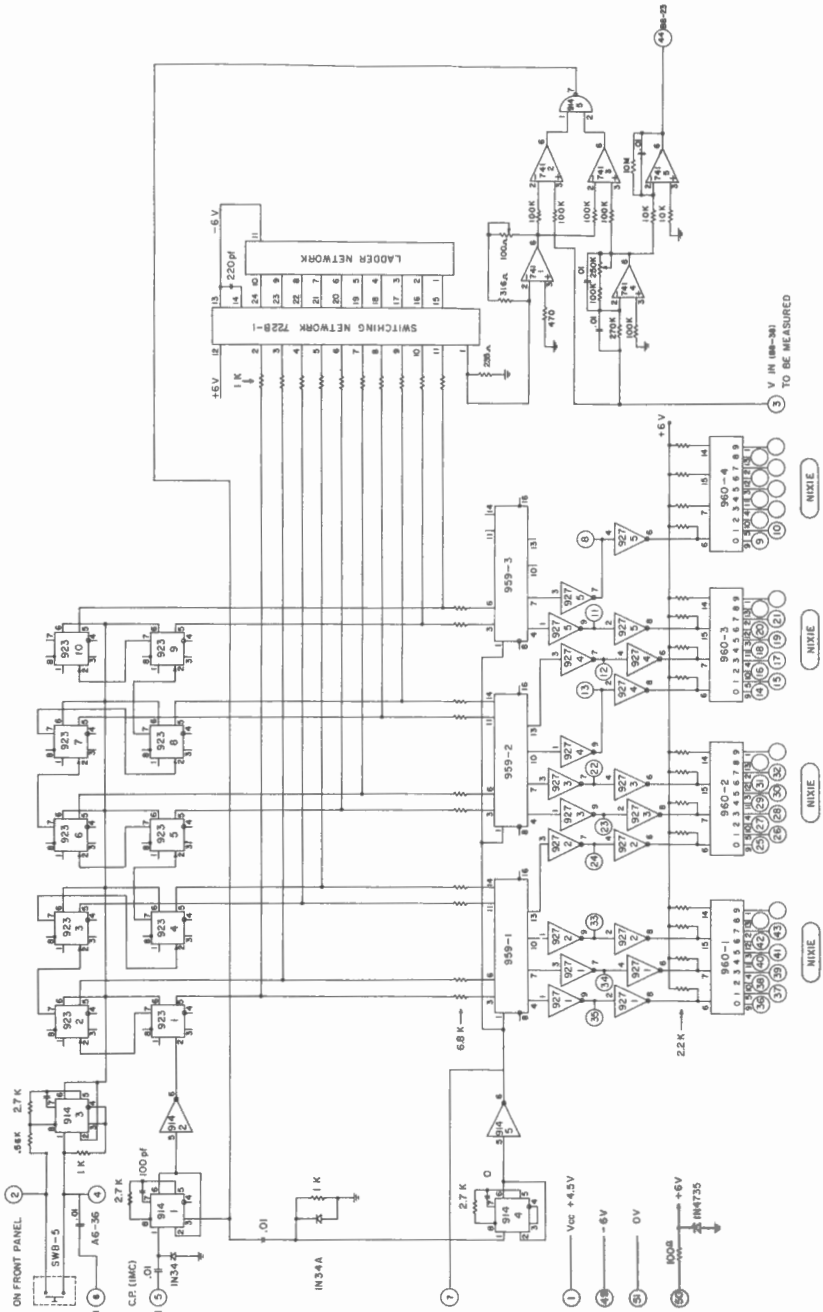


Figure 41. The digital volt meter logic diagram.

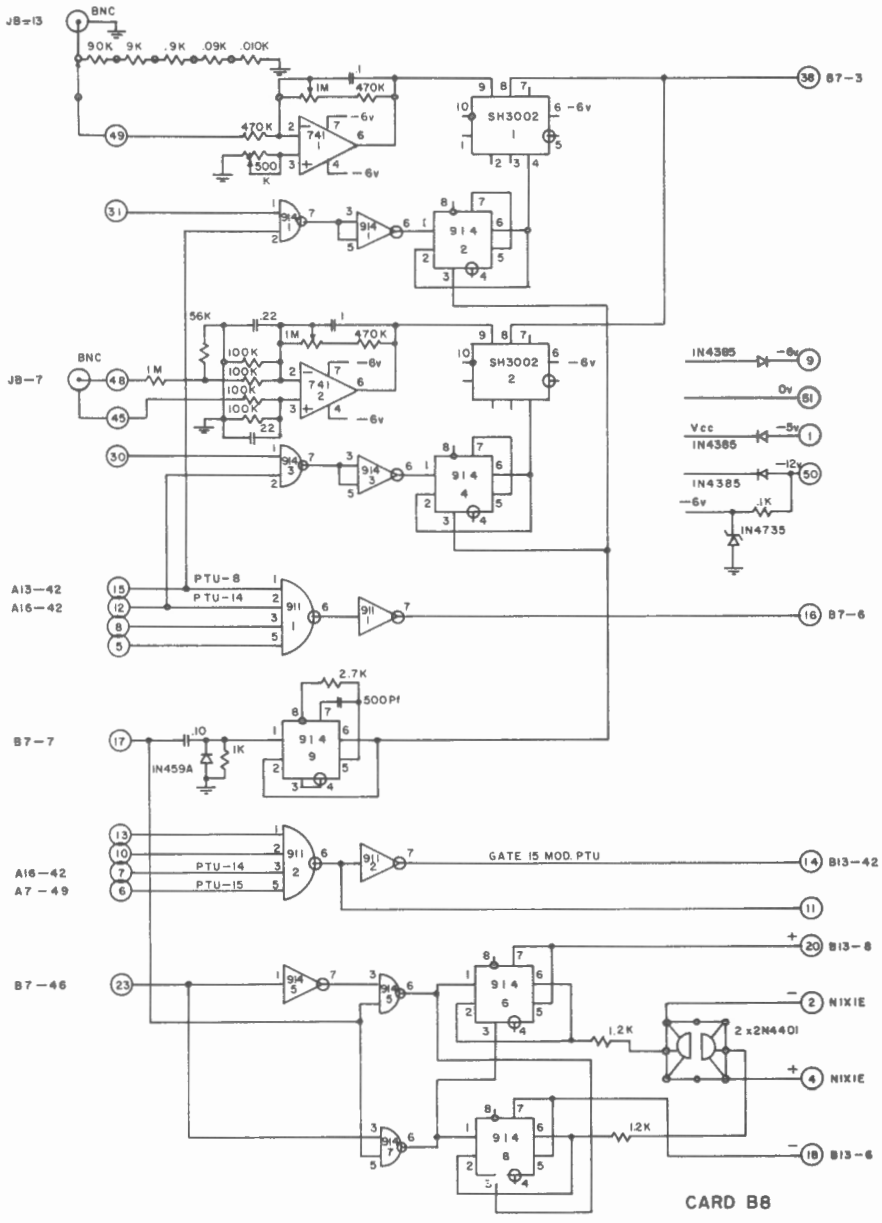
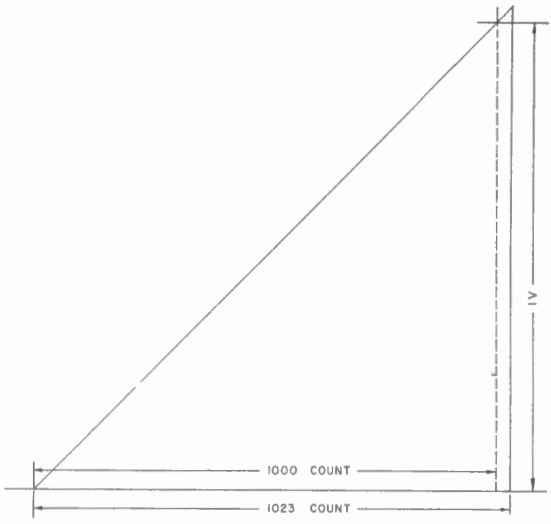
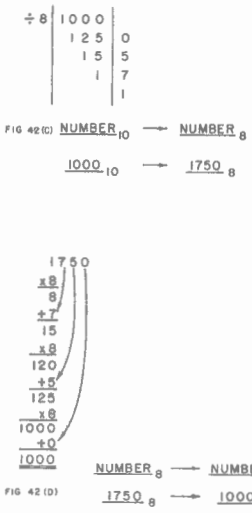


Figure 41A. Digital volt meter multiplexer.





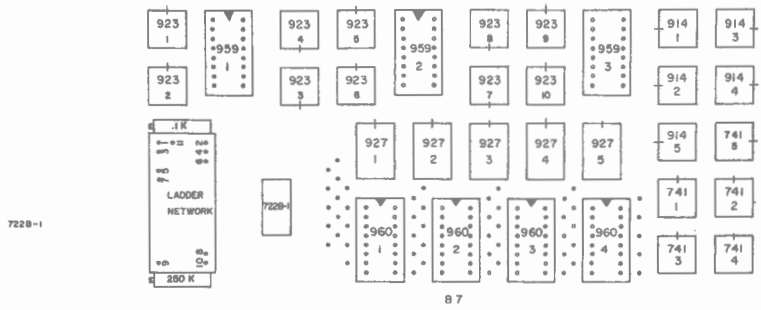
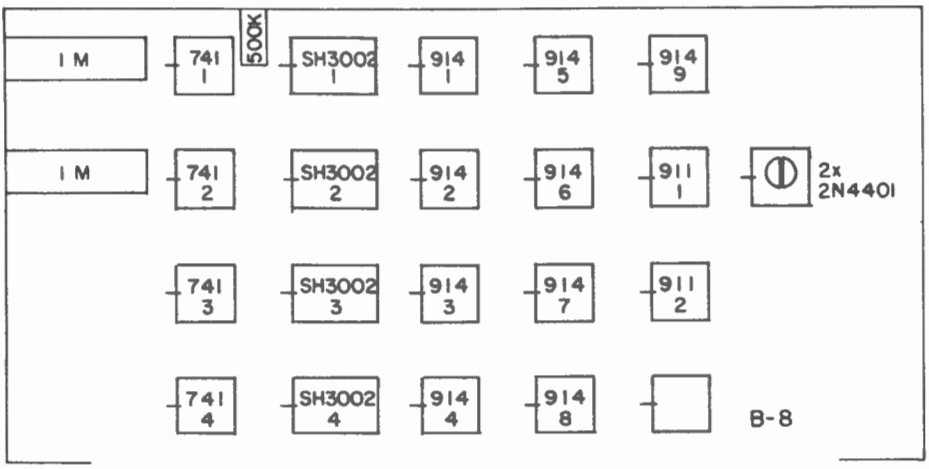


Figure 42. The digital volt meter card layout, calibration diagram and conversion examples.



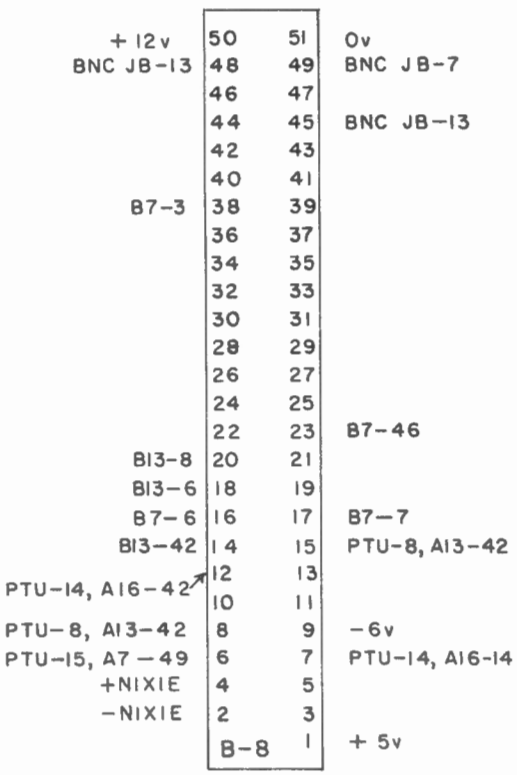


Figure 42B. Digital volt meter multiplexer card layout.

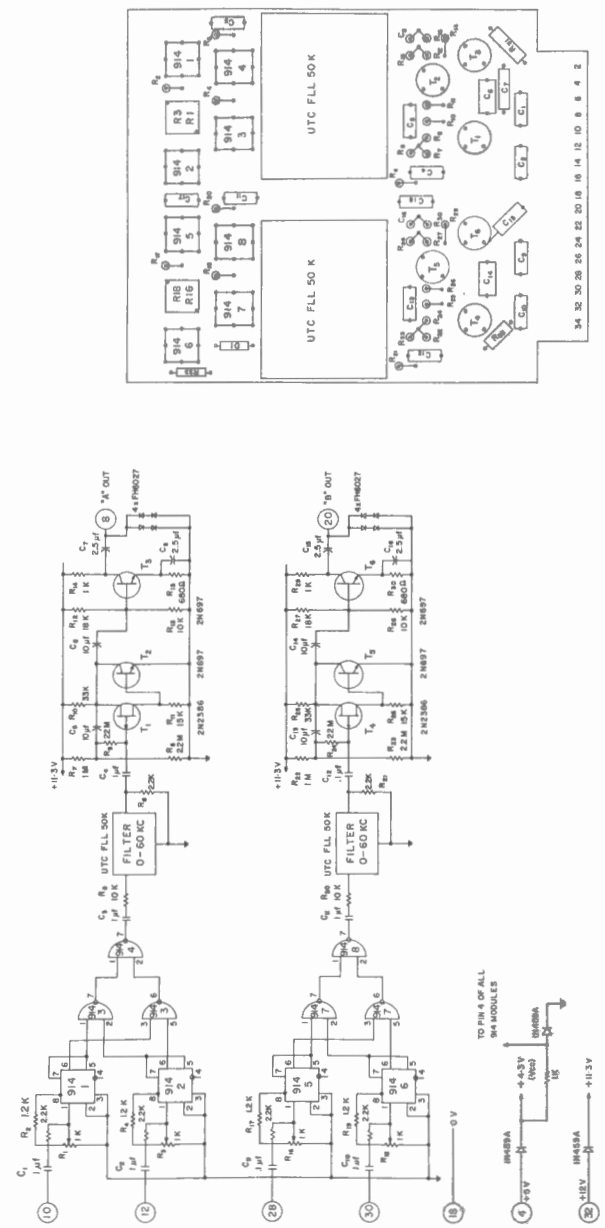


Figure 43. The Mixer and low pass filter logic diagram and component layout.

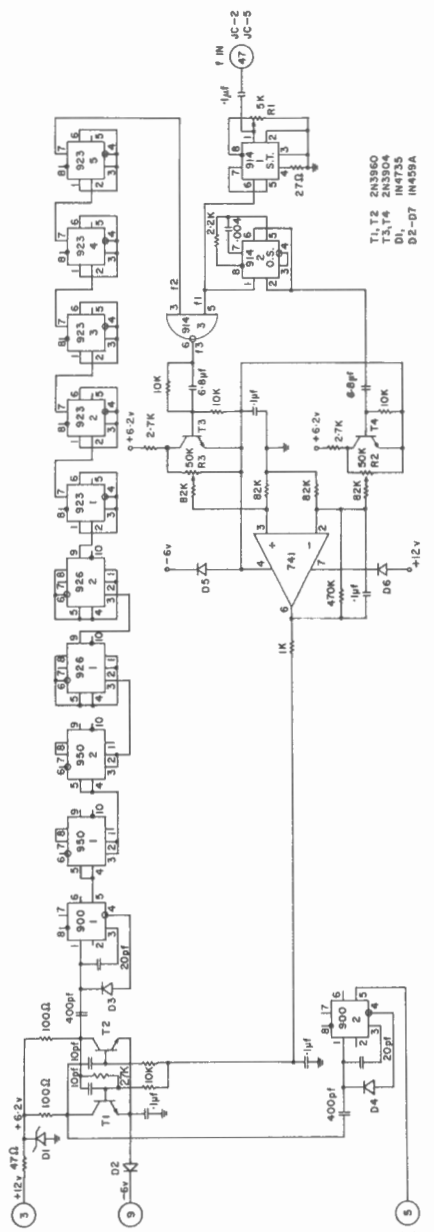


Figure 44A. The phase lock tracking filter logic diagram.

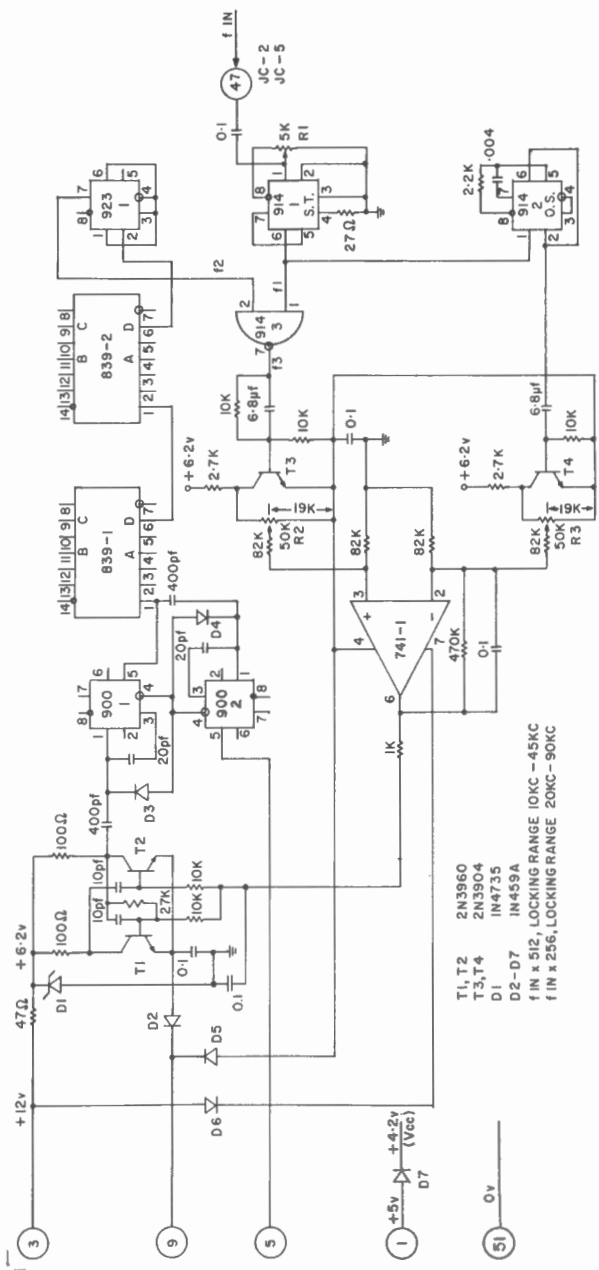


Figure 44B. The phase lock tracking filter logic diagram.

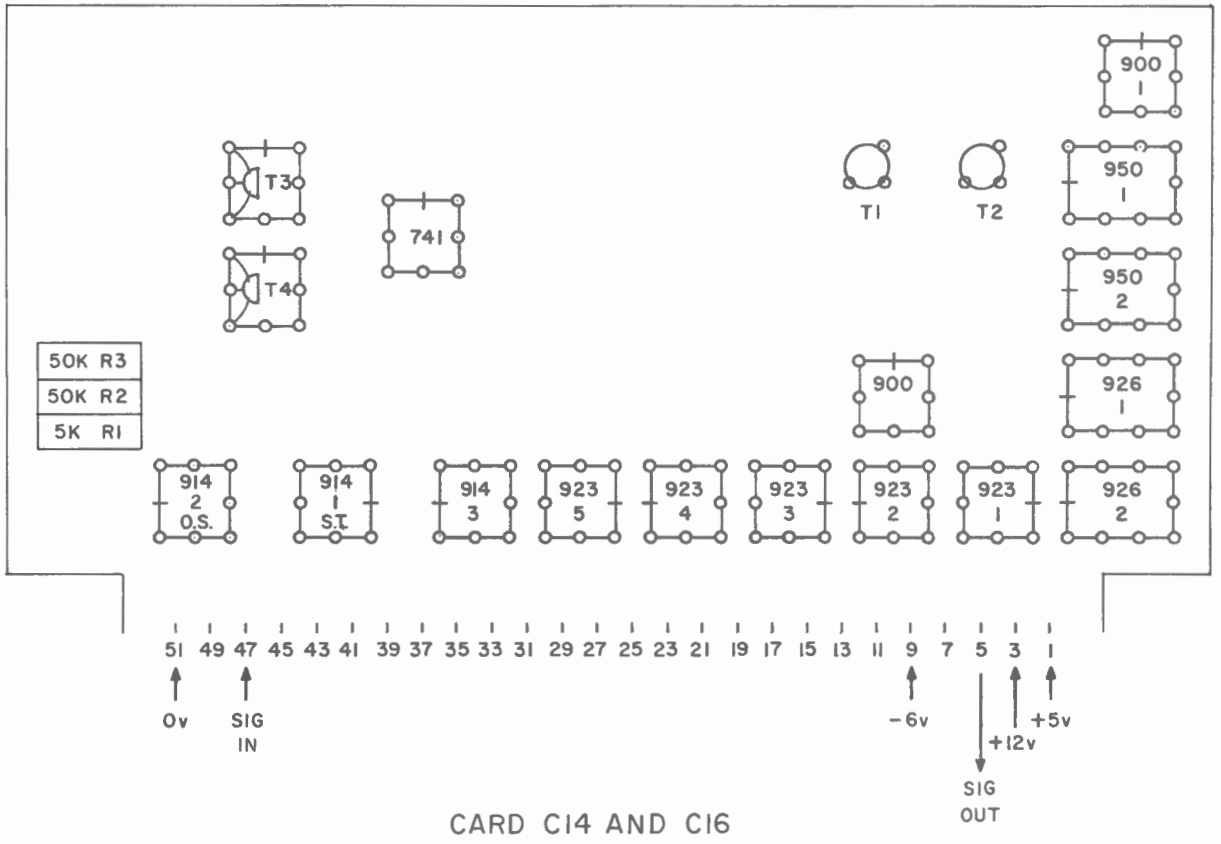


Figure 45A. The phase lock tracking filter card layout.

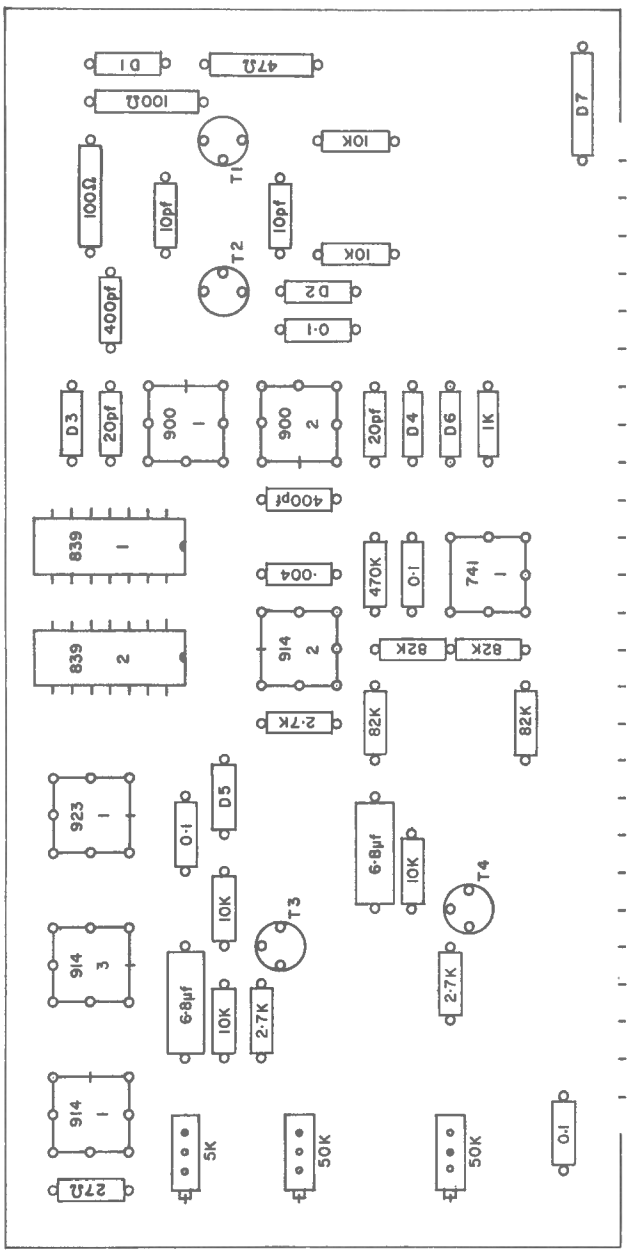


Figure 45B. The phase lock tracking filter card layout.

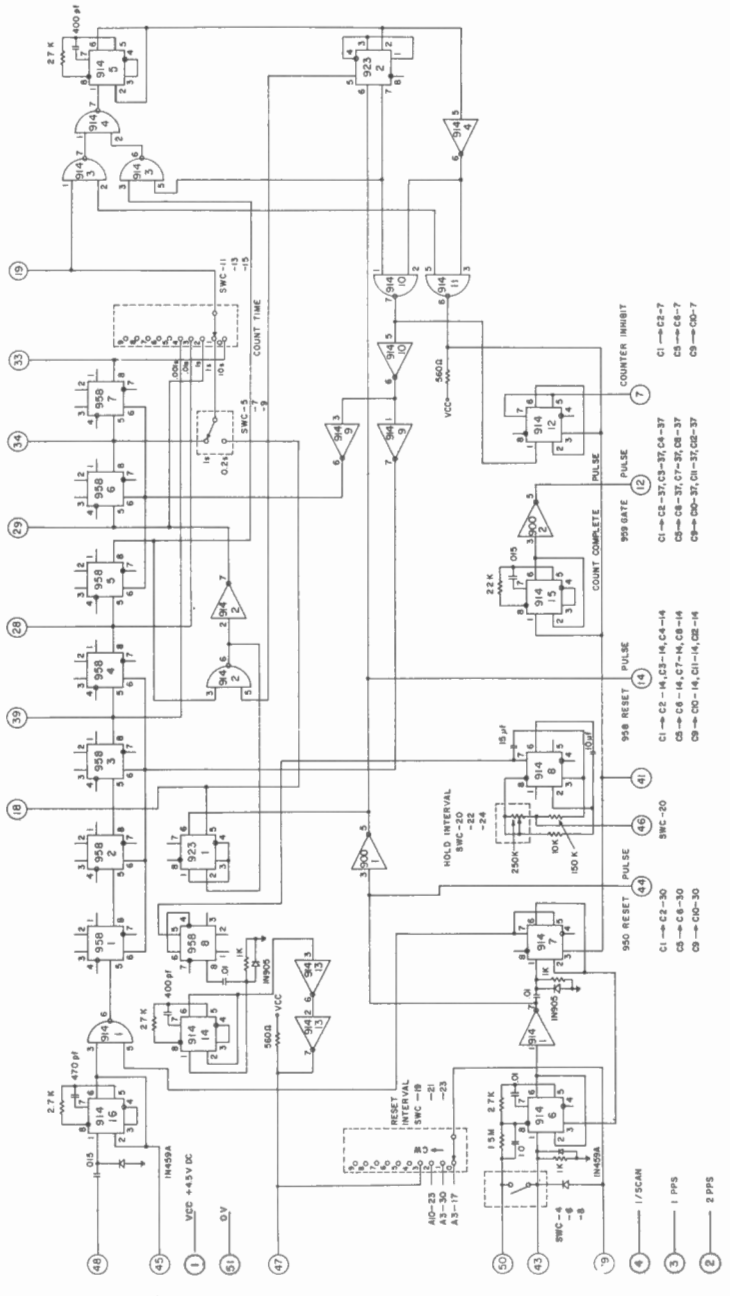


Figure 46. The high speed counter control card.

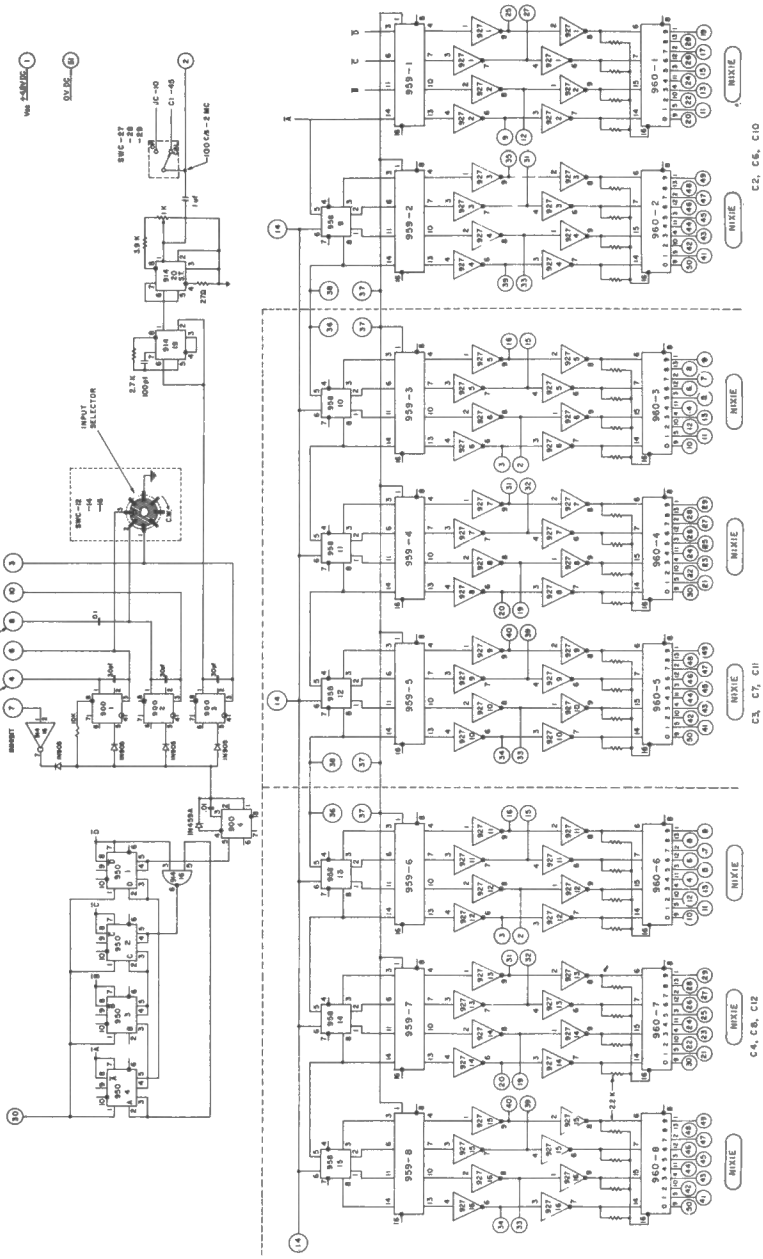


Figure 47. The high speed counter input and display logic.

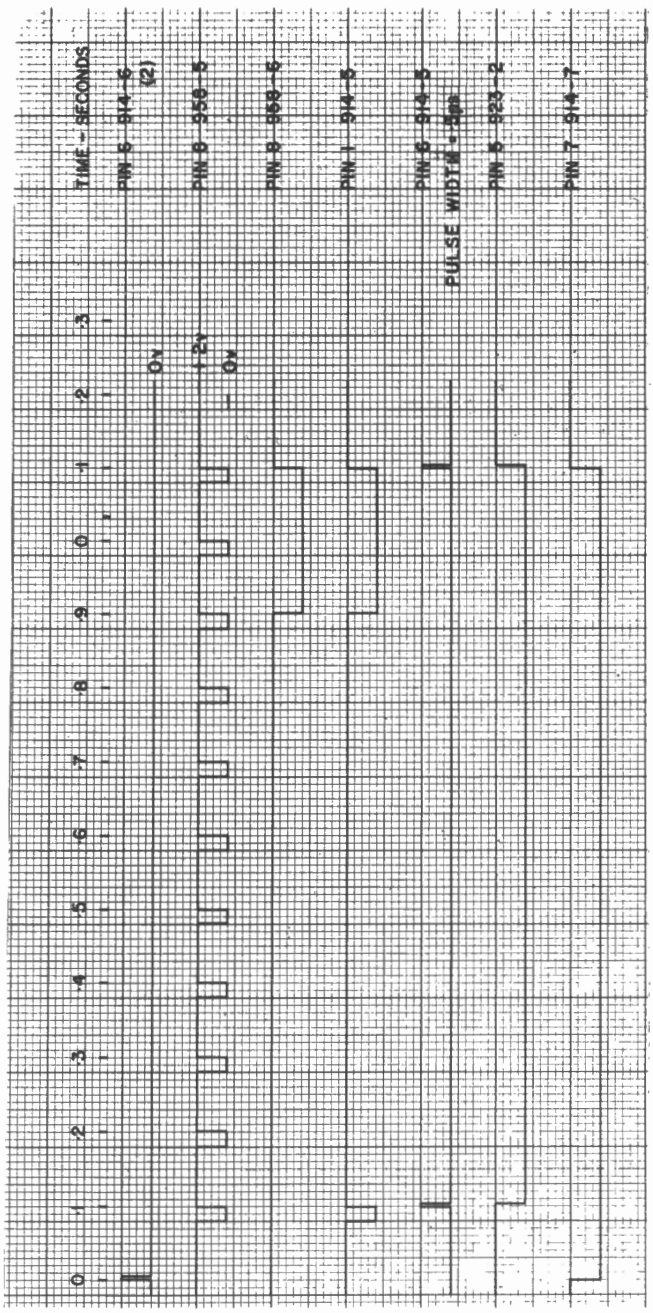


Figure 48. The high speed counter timing diagram.

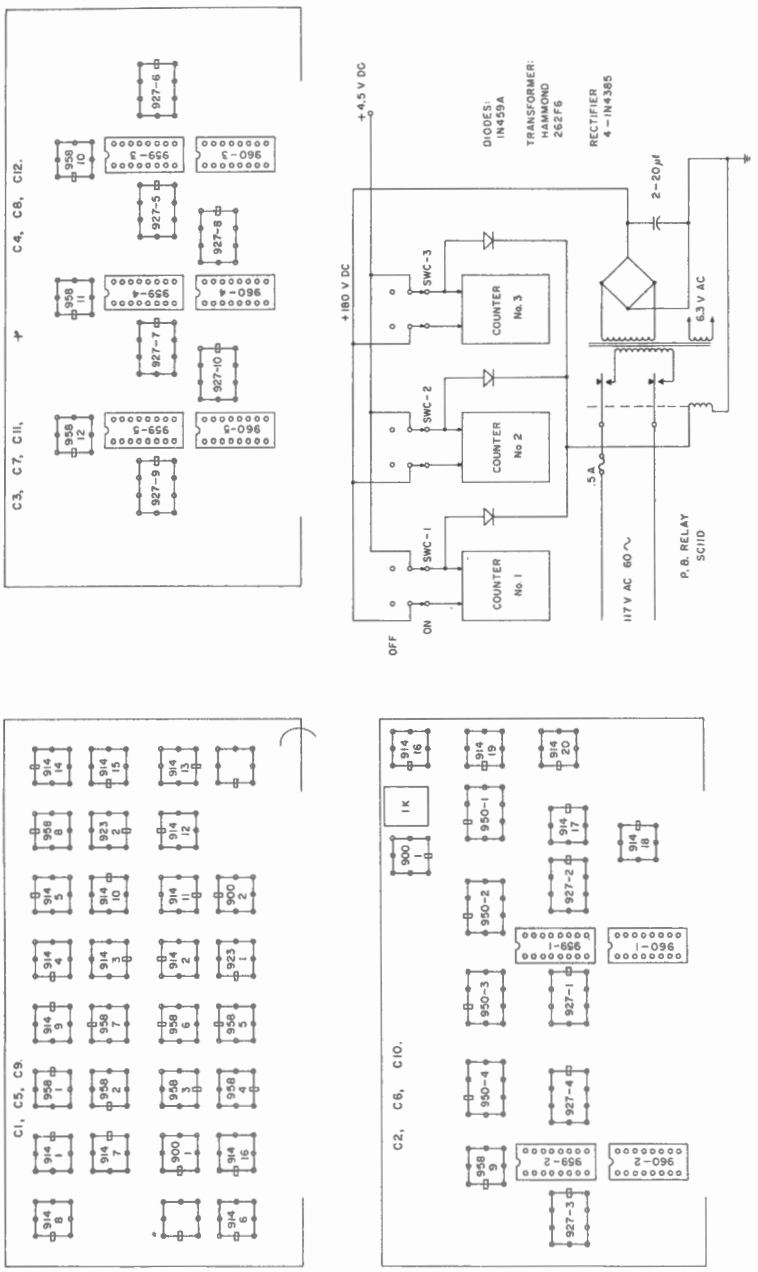


Figure 49. The high speed counter card layout and control diagram for the low and high voltage.

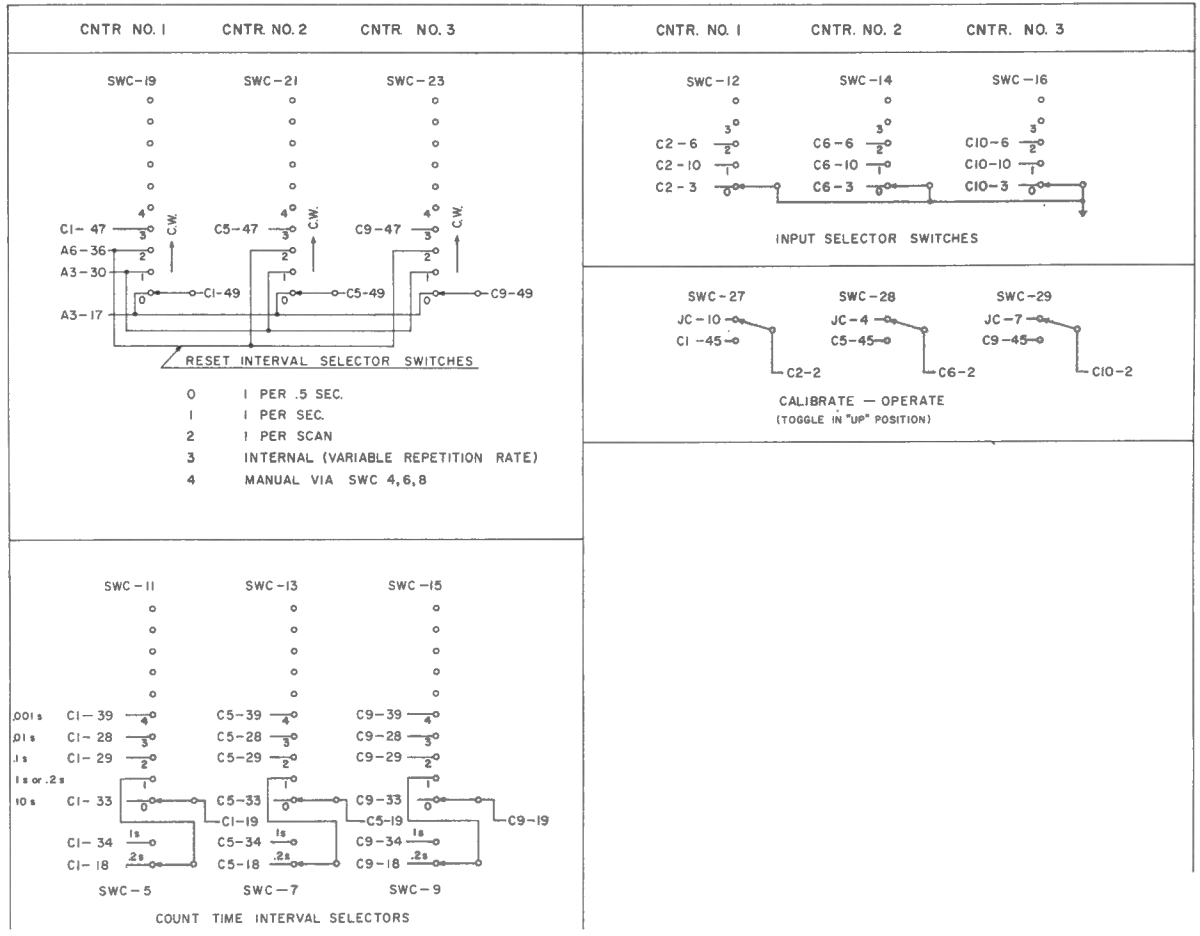


Figure 50. Control switching for the counters.

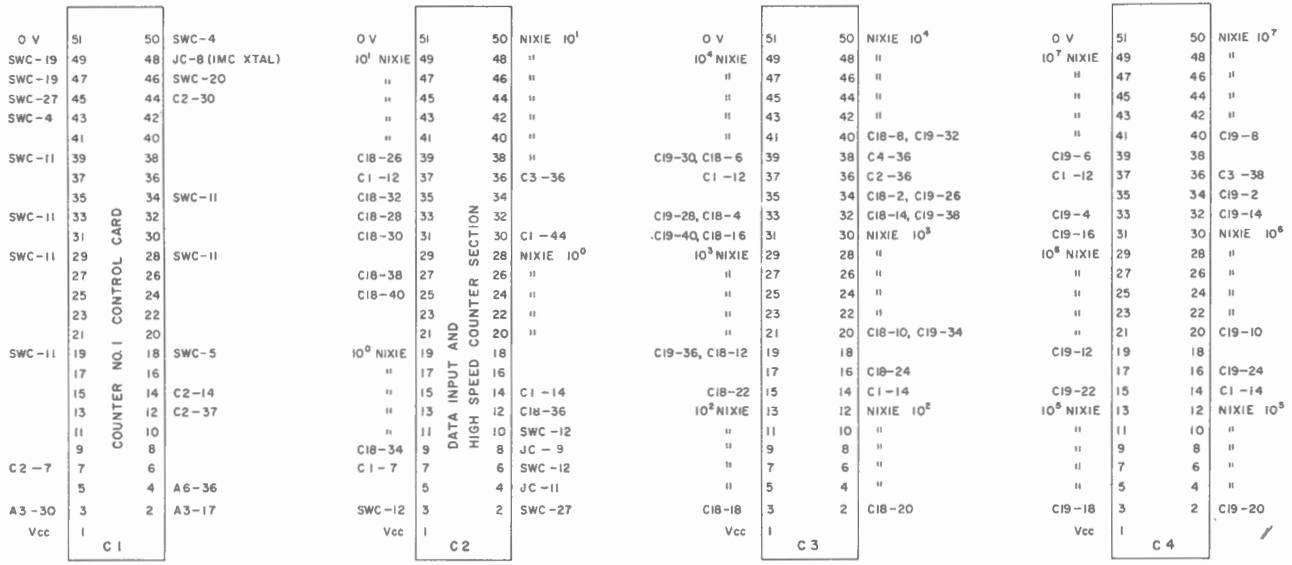


Figure 51. Intercard wiring for high speed counter No. 1.

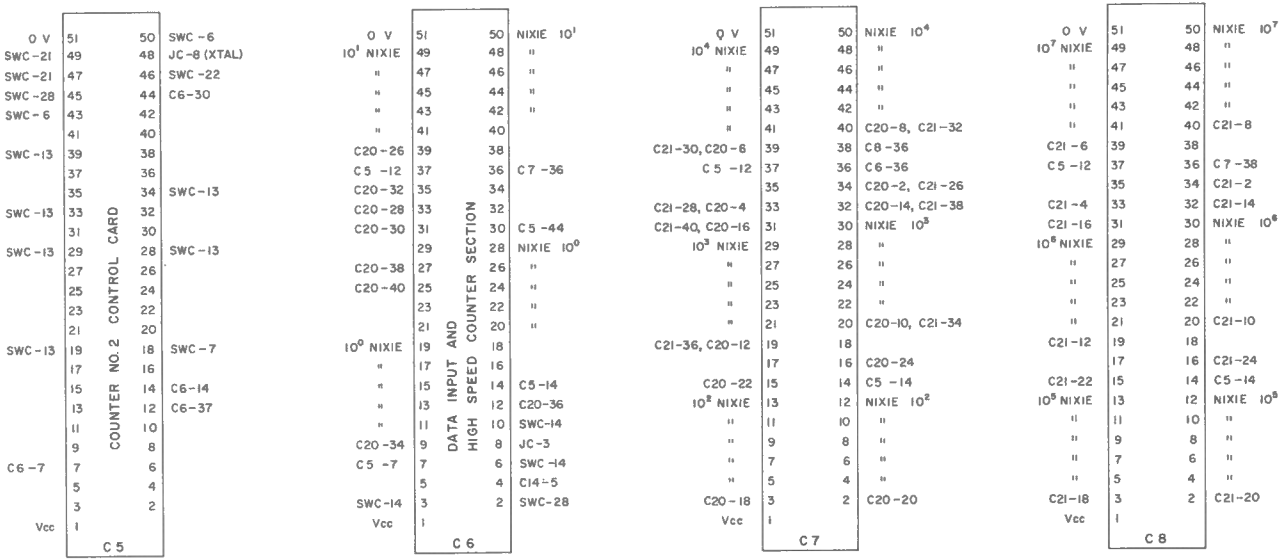


Figure 52. Intercard wiring for high speed counter No. 2.

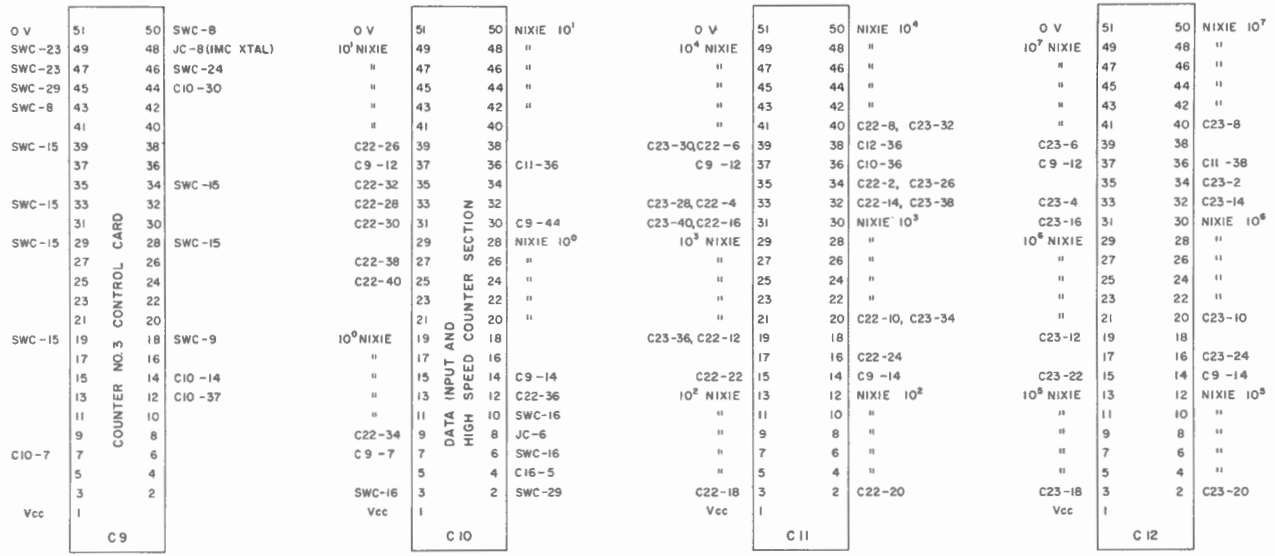


Figure 53. Intercard wiring for high speed counter No. 3.

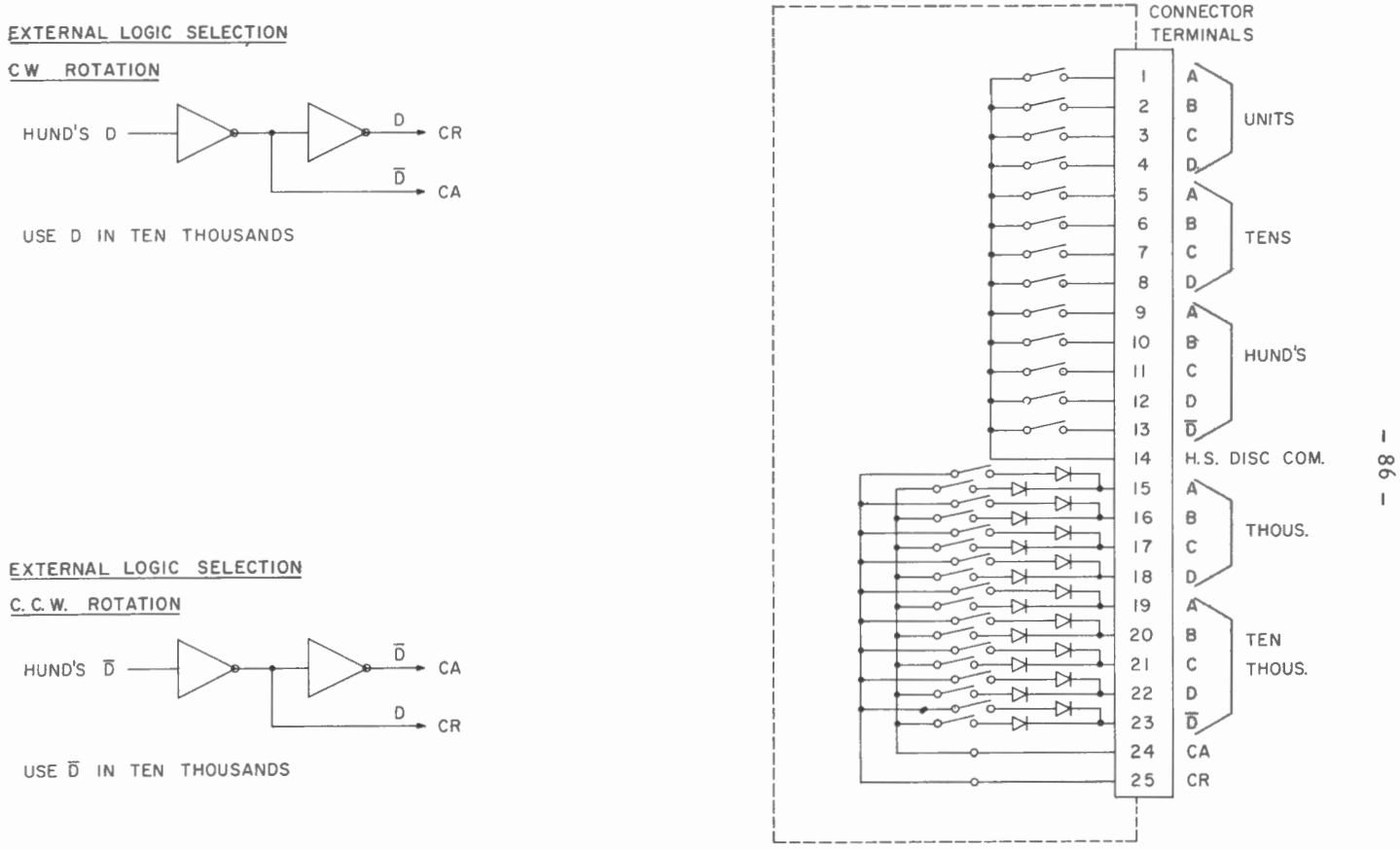


Figure 54. The shaft position encoder functional schematic.

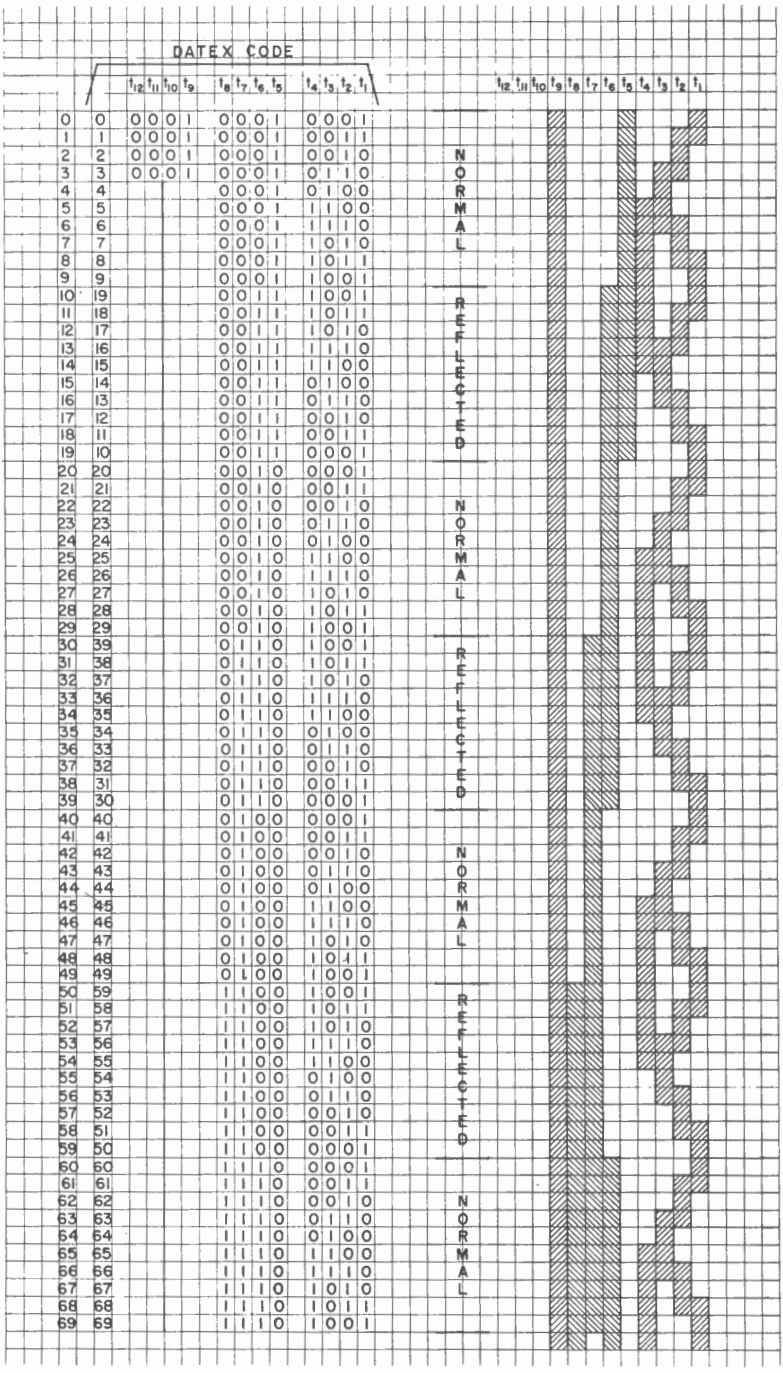
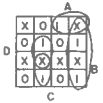


Figure 55. The contact arrangement for the Datex encoders.

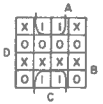
DATEX TO 8421

NO.	A	B	C	D	DATEX	8	4	2	1
0	0	0	0	0	X	X	X	X	X
1	0	0	0	1	0	0	0	0	0
2	0	0	1	0	2	0	0	1	0
3	0	0	1	1	1	0	0	0	1
4	0	1	0	0	4	0	1	0	0
5	0	1	0	1	X	X	X	X	X
6	0	1	1	0	3	0	0	1	1
7	0	1	1	1	X	X	X	X	X
8	1	0	0	0	X	X	X	X	X
9	1	0	0	1	9	1	0	0	1
10	1	0	1	0	7	0	1	1	1
11	1	0	1	1	8	1	0	0	0
12	1	1	0	0	5	0	1	0	1
13	1	1	0	1	X	X	X	X	X
14	1	1	1	0	6	0	1	1	0
15	1	1	1	1	X	X	X	X	X

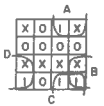


1 = $A\bar{C} + A\bar{B}\bar{D} + \bar{A}BC + \bar{A}CD$

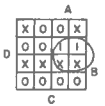
$= A(\bar{C} + \bar{B}\bar{D}) + \bar{A}C(B + D)$



2 = $C\bar{D}$



4 = $A\bar{D} + B\bar{C}$



8 = AD

CORRECTION FOR REFLECTED PORTION OF DATEX CARD

DATEX CODE →	A	B	C	D	m
N 0	0	0	0	1	1
R 1	0	0	1	1	3
N 2	0	0	1	0	2
R 3	0	1	1	0	6
N 4	0	1	0	0	4
R 5	1	1	0	0	12
N 6	1	1	1	0	14
R 7	1	0	1	0	10
N 8	1	0	1	1	11
R 9	1	0	0	1	9
X X	0	0	0	0	0
X X	0	1	0	1	5
X X	0	1	1	1	7
X X	1	0	0	0	8
X X	1	1	0	1	13
X X	1	1	1	1	15

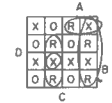
$t_4\ t_3\ t_2\ t_1$

$t_8\ t_7\ t_6\ t_5$

$t_{12}\ t_{11}\ t_{10}\ t_9$

$t_{16}\ t_{15}\ t_{14}\ t_{13}$

$t_{20}\ t_{19}\ t_{18}\ t_{17}$



R = $A\bar{C} + A\bar{B}\bar{D} + \bar{A}BC + \bar{A}CD$

$= A(\bar{C} + \bar{B}\bar{D}) + \bar{A}C(B + D)$

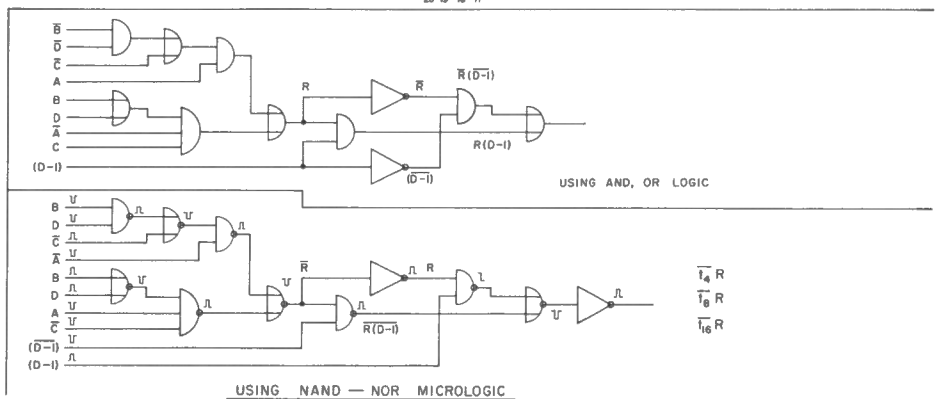


Figure 56. Manipulation of the Datex code.

DATEX CODE TO 8421

1 ST DIGIT	1	$A(\overline{C}+\overline{B}\overline{D})+\overline{A}C(B+D)$	$= t_{4R}(\overline{t_2}+\overline{t_3}\overline{t_1})+\overline{t_{4R}}t_2(t_3+t_1)$
10^0	2	$C\overline{D}$	$= t_2\overline{t_1}$
	4	$A\overline{D}+B\overline{C}$	$= t_{4R}\overline{t_1}+t_3\overline{t_2}$
	8	AD	$= t_{4R}t_1$
2 ND DIGIT	1	$t_{8R}(\overline{t_6}+\overline{t_7}\overline{t_5})+\overline{t_{8R}}t_6(t_7+t_5)$	
10^1	2	$t_6\overline{t_5}$	
	4	$t_{8R}\overline{t_5}+t_7\overline{t_6}$	
	8	$t_{8R}t_5$	
3 RD DIGIT	1	$t_{12}(\overline{t_{10}}+\overline{t_{11}}\overline{t_9})+\overline{t_{12}}t_{10}(t_{11}+t_9)$	
10^2	2	$t_{10}\overline{t_9}$	
	4	$t_{12}\overline{t_9}+t_{11}\overline{t_{10}}$	
	8	$t_{12}t_9$	
4 TH DIGIT	1	$t_{16R}(\overline{t_{14}}+\overline{t_{15}}\overline{t_{13}})+\overline{t_{16R}}t_{14}(t_{15}+t_{13})$	
10^3	2	$t_{14}\overline{t_{13}}$	
	4	$t_{16R}\overline{t_{13}}+t_{15}\overline{t_{14}}$	
	8	$t_{16R}t_{13}$	
5 TH DIGIT	1	$t_{20}(\overline{t_{18}}+\overline{t_{19}}\overline{t_{17}})+\overline{t_{20}}t_{18}(t_{19}+t_{17})$	
10^4	2	$t_{18}\overline{t_{17}}$	
	4	$t_{20}\overline{t_{17}}+t_{19}\overline{t_{18}}$	
	8	$t_{20}t_{17}$	

Figure 57. The Boolean equations for a five number display.

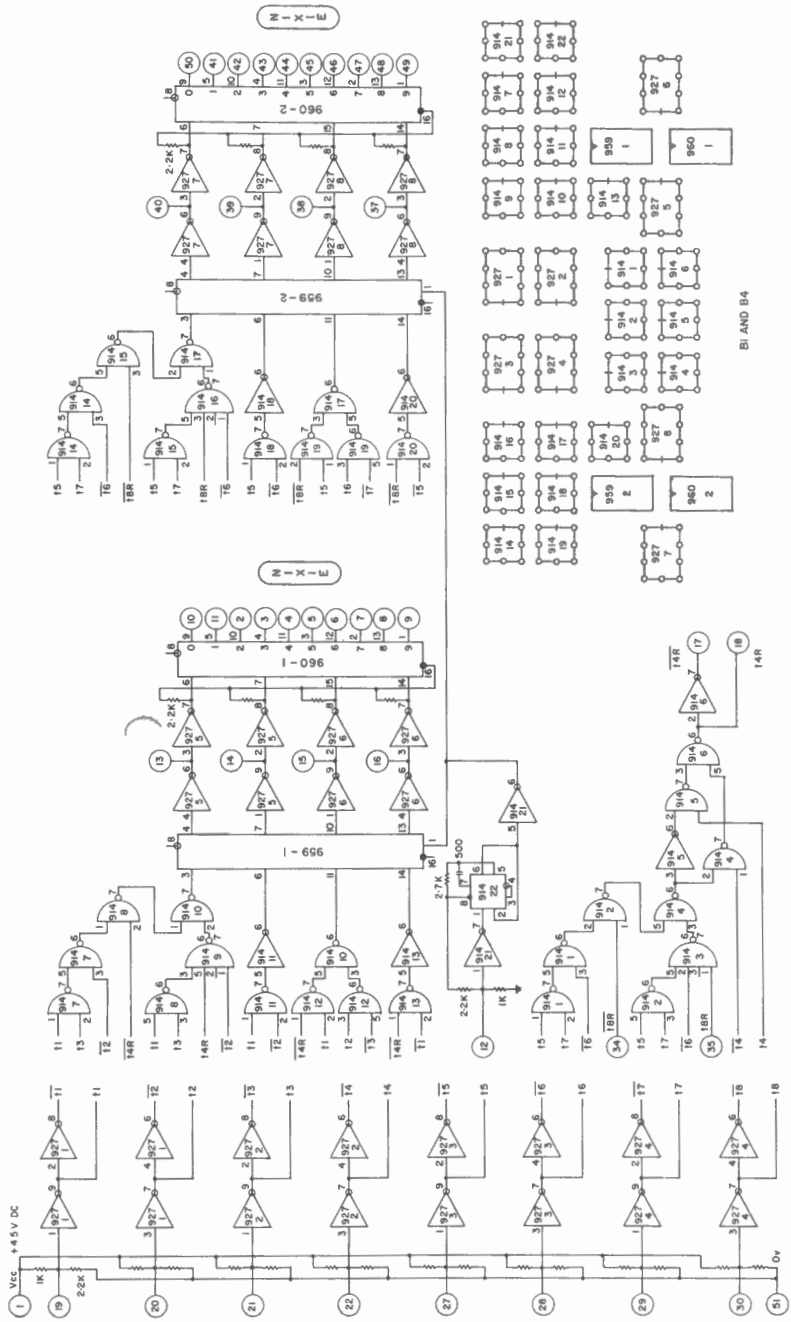


Figure 58. 10° Decoder logic and card layout.

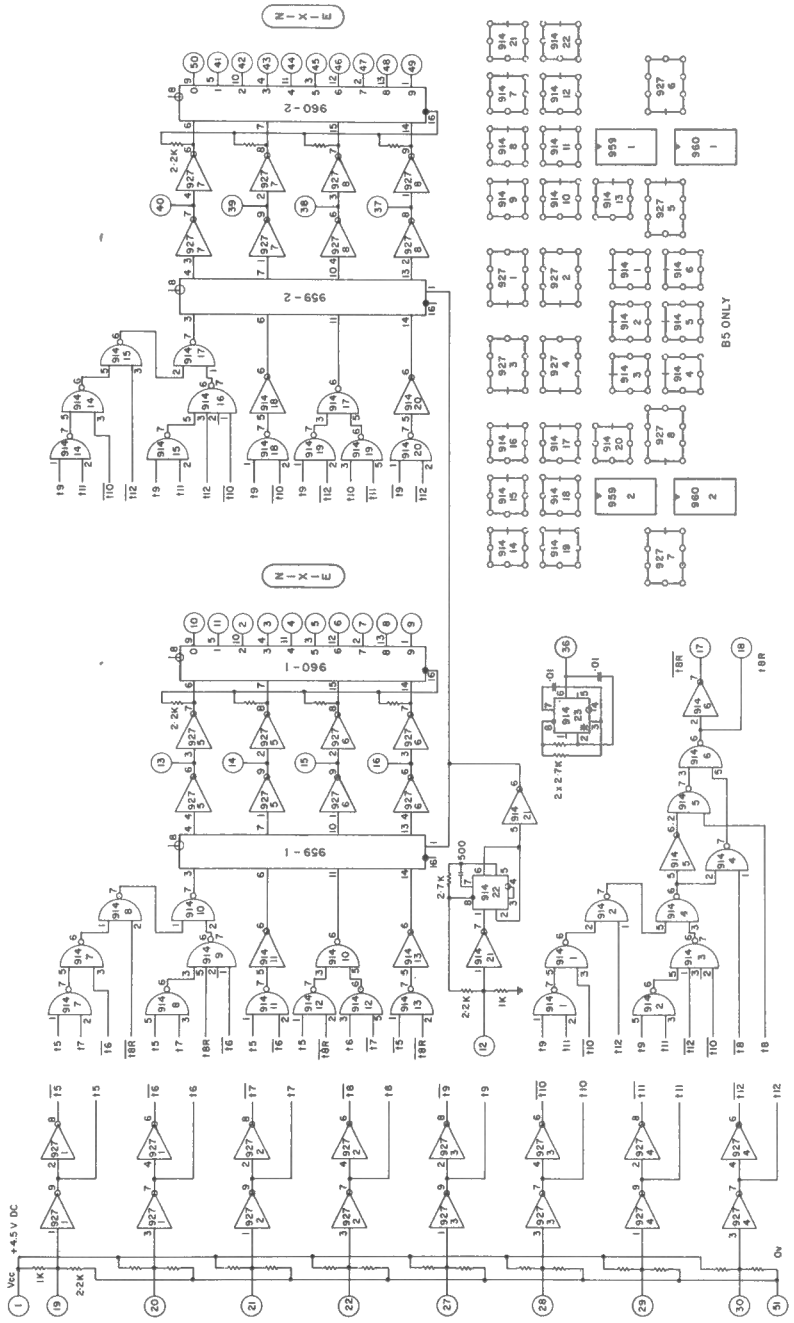


Figure 59. 10^1 and 10^2 Decoder logic and card layout.

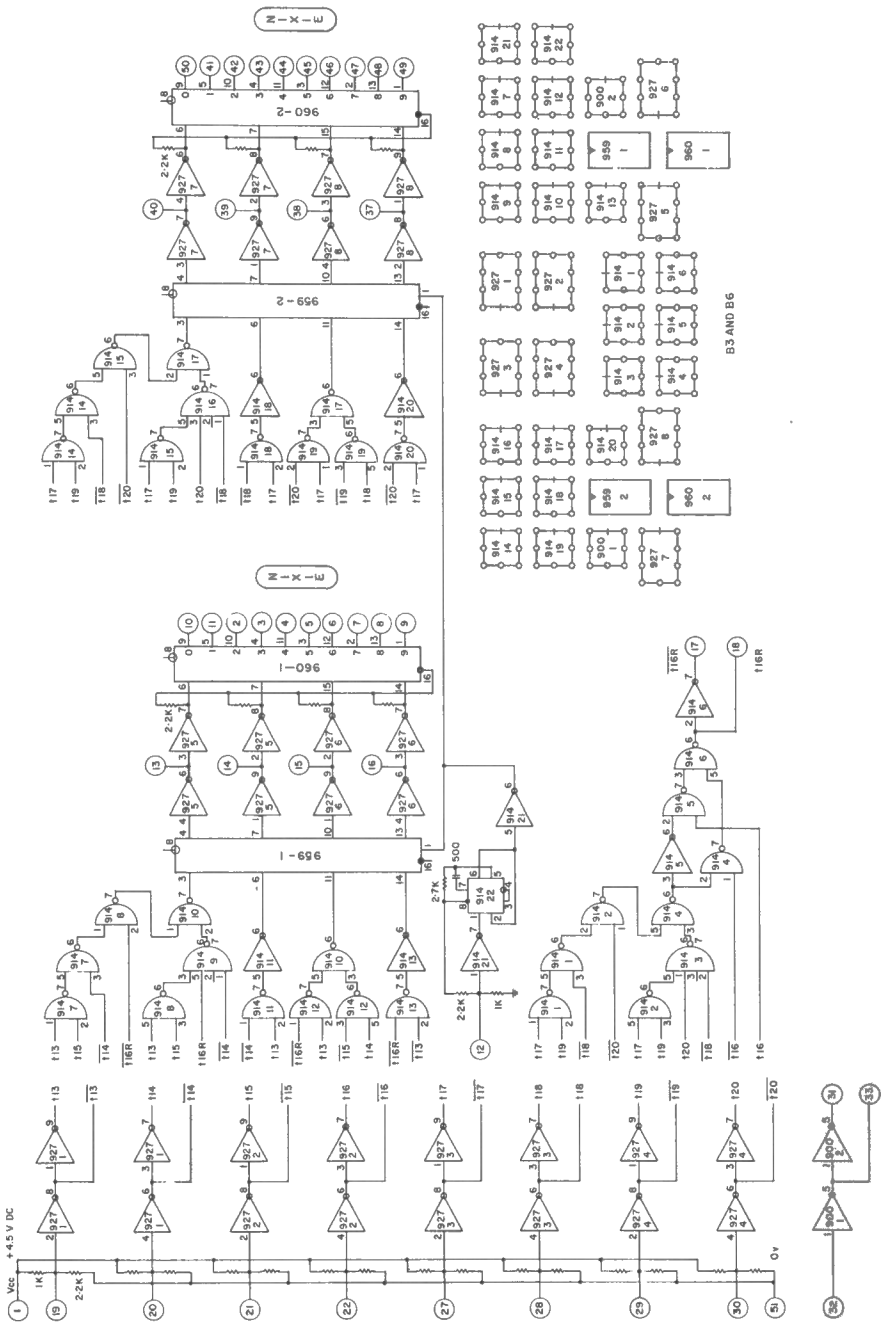


Figure 60. 10^3 and 10^4 Decoder logic and card layout.

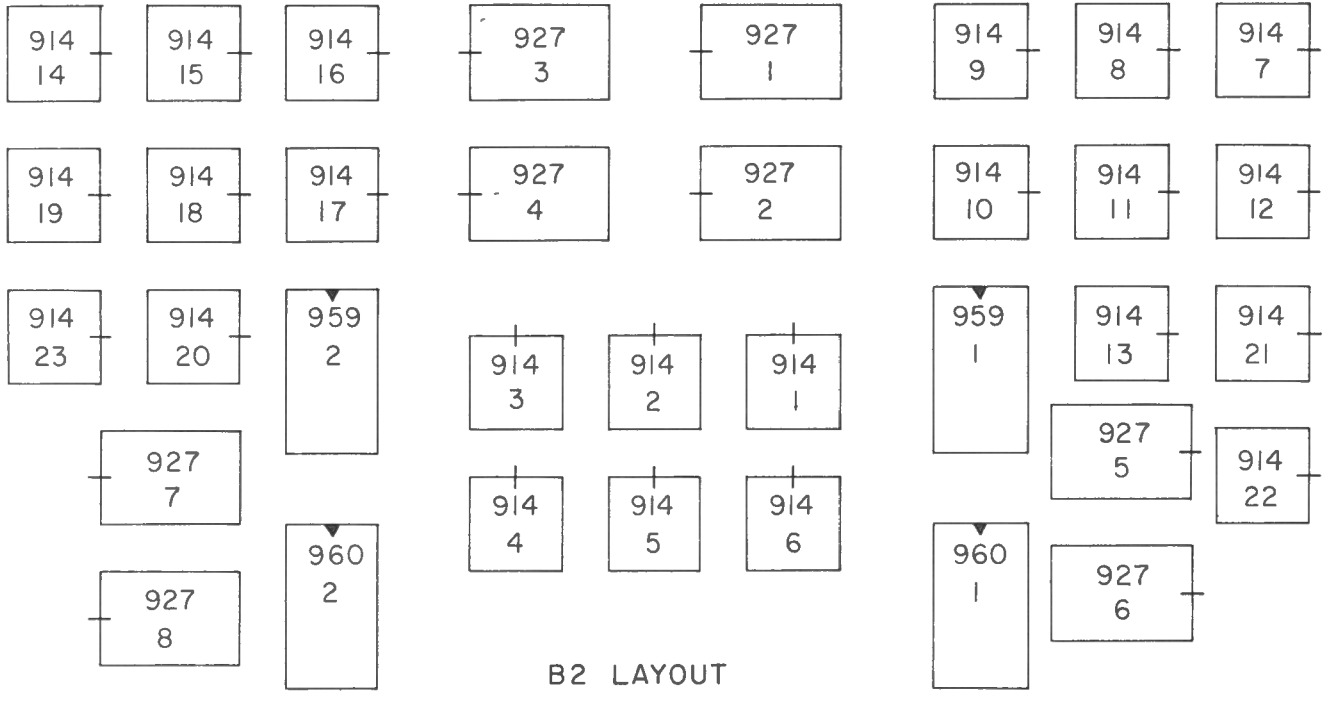


Figure 61. The card layout of B2 only.

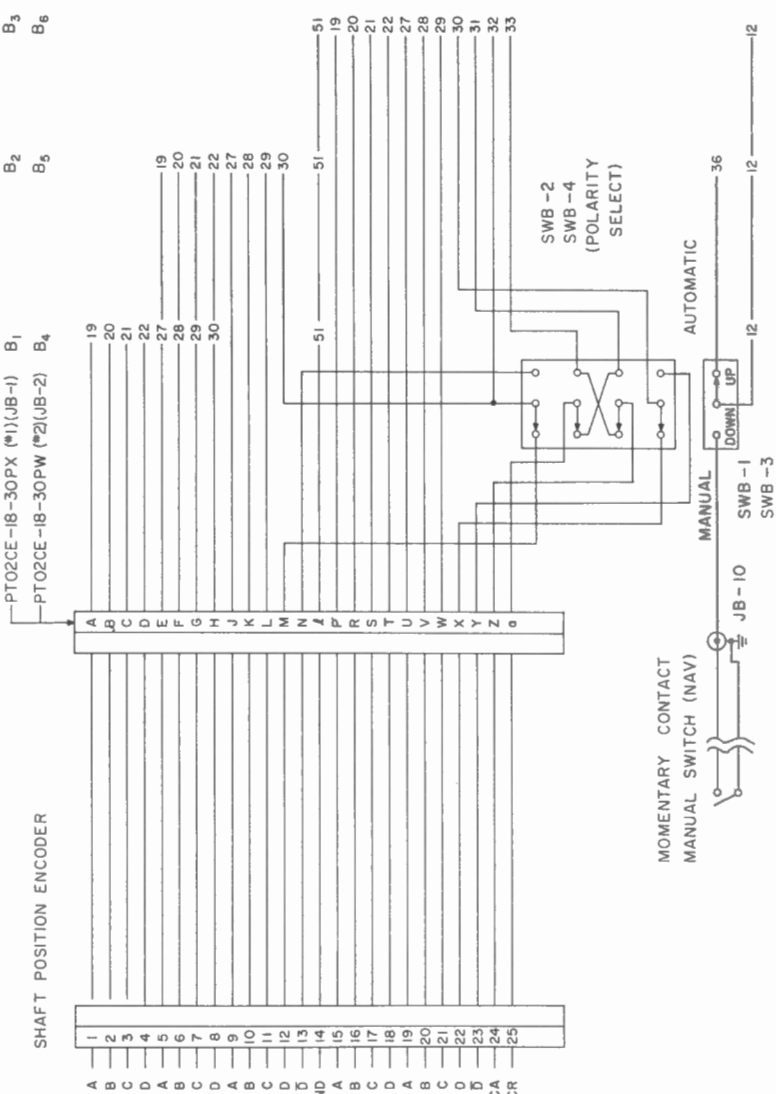


Figure 62. The input cabling the shaft position decoder logic.

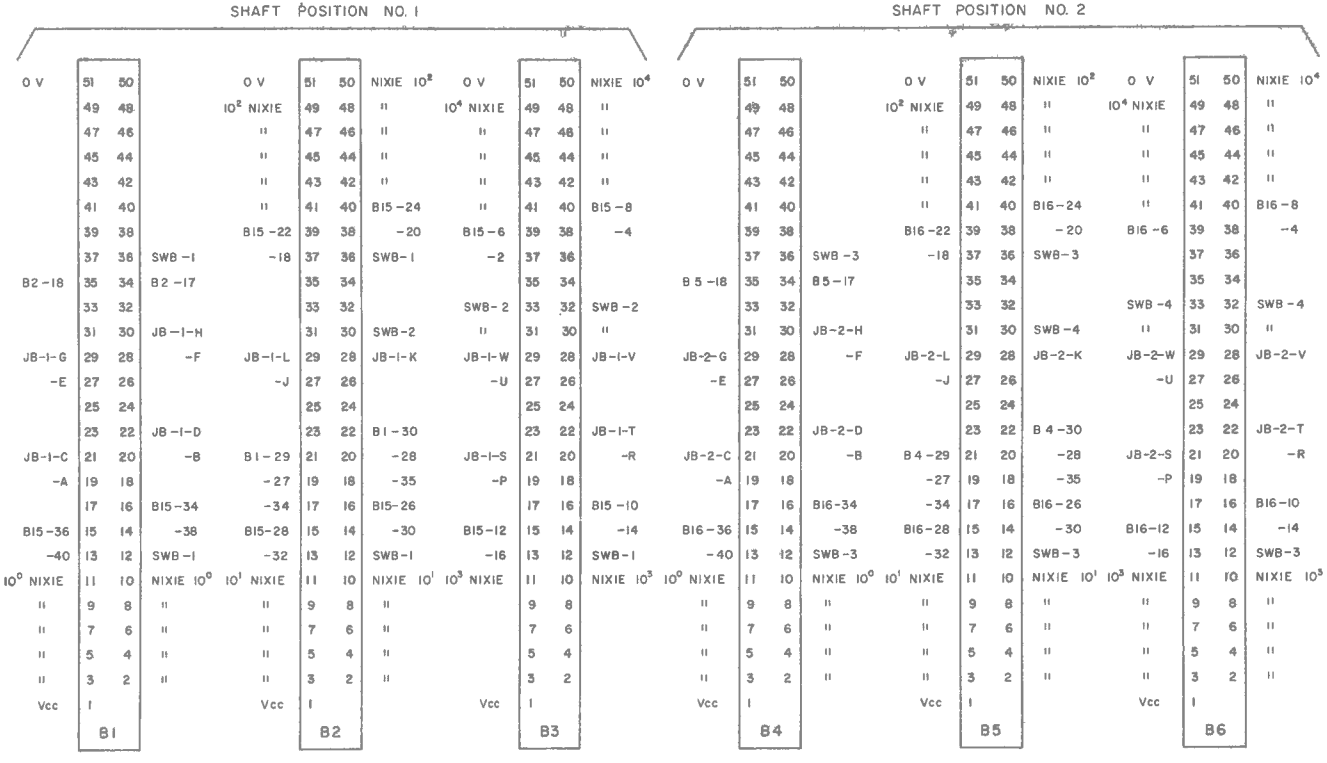


Figure 63. The intercard wiring for the shaft position decoder logic cards, units No. 1 and No. 2.